Intel® 845GV Scalable Performance Board

Development Kit User's Manual

February 2003

Order Number: 273830-001

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

Contents

1 About This Manual 7

1.1 Content Overview 7
1.2 Text Conventions 8
1.3 Support Options 9
1.3.1 Electronic Support Systems 9
1.4 Product Literature 9
1.5 Related Documents 10

2 Getting Started 11

2.1 Overview 11
2.1.1 Baseboard Features 11
2.2 Included Hardware 13
2.3 Software Key Features 13
2.3.1 AMI BIOS 13
2.3.2 Windows XP Embedded* (CD Included) 14
2.4 Before You Begin 15
2.5 Setting Up the Evaluation Board 16
2.6 Configuring the BIOS 18

3 Theory of Operation 19

3.1 Block Diagram 19
3.2 Major Features 20
3.3 Mechanical Diagram 21
3.4 Thermal Management 21
3.5 System Operation 21
3.5.1 Intel® Celeron® processor 22
3.5.2 Intel® Pentium® 4 Processor 22
3.5.3 Intel® 845GV Chipset 24
3.5.3.1 Graphics and Memory Controller Hub (GMCH) 24
3.5.3.2 Hub Interface 24
3.5.3.3 I/O Controller Hub (ICH4) 25
3.5.3.4 Firmware Hub (FWH) 25
3.5.4 System Memory 26
3.5.4.1 DDR SDRAM 26
3.5.4.2 PC133 SDRAM 26
3.5.5 Boot ROM 26
3.5.6 System I/O 26
3.5.6.1 PCI-LAN- USB-Audio 27
3.5.6.2 Floppy Disk Drive Support 27
3.5.6.3 IDE Support 27
3.5.6.4 RS-232 Serial Ports 27
3.5.6.5 IEEE 1284 Parallel Port 27
3.5.6.6 USB Ports 27
3.5.6.7 VGA Connector 28
3.5.6.8 Audio Subsystem 28
3.5.6.9 Keyboard/Mouse 28
3.5.7 Expansion Connectors 28

3.5.7.1 32-bit/33-MHz PCI Connectors 28
3.5.7.2 CNR Connectors 28
3.5.8 Voltage Monitoring 28
3.5.9 Post Code Debugger 28
3.5.10 Clock Generation 28
3.5.10.1 System Clocks 29
3.6 Power Management Model 29
3.6.1 Power Supply Requirements 29
3.6.2 Transition to S1 or S3 29
3.6.3 Transition to S4 29
3.6.4 Transition to S5 29
3.6.5 Transition to Full-On 30
3.7 Battery Requirements 30

4 Hardware Reference 31

4.1 Thermal Management 31
4.2 Board Debugging 31
4.2.1 In Target Probe (ITP) 31
4.2.2 USB Debug Port 31
4.2.3 Port 80h 31
4.2.4 Digital Video Debug Port 32
4.2.5 Board Mounted Power Control and Reset Switches 32
4.2.6 Power LEDs 33
4.3 Connector Pinouts 33
4.4 Jumper Functions 34
4.5 Header Functions 35
4.5.1 ATX12V Power Connector 36
4.5.2 Enhanced IDE Pinout 37
4.5.2.1 Fan Connectors 37
4.5.3 COM Ports 38
4.5.4 VGA Adapter Connector 38
4.6 LED Functions 39

5 BIOS Information 41

A Bill Of Materials 43

B Schematics 57

Figures

1 Block Diagram 19
2 Back Panel I/O Connectors 27
3 Motherboard Layout 33

Tables

1 Related Documents 10
2 Feature Table 20
3 Digital Video Debug Port Connector (J6C1) 32

4 Jumper Definitions 34
5 Header Definitions 35
6 Power Connector (J2J3) 36
7 +12V Power Connector (J5C1) 36
8 EIDE Connector Pinout (J6H1 and J6H2) 37
9 Fan Connectors 37
10 COM Ports 38
11 VGA Adapter Connector (J1H1) 38
12 LED Definitions 39
13 Bill of Materials for Intel Manufactured Parts 43
14 Bill of Materials for Third Party Manufactured Parts 43

Revision History

Date	Revision	Description
February 2003	001	Initial release of this document

About This Manual 1

This user's manual describes the use of the Intel® Celeron® processor in the 478 Pin Package and Intel® 845GV Chipset development kit. This manual has been written for OEMs, system evaluators and network appliance developers. All jumpers, headers, and LED functions and their locations on the board, along with subsystem features and POST codes, are defined in this document. The design schematics are at the end of this document.

For the latest information about the Intel® 845GV Scalable Performance Board reference platform, visit:

http://developer.intel.com/design/intarch/devkits/index.htm

Features of the scalable reference platform include:

- Scalable performance using the Intel® Pentium® 4 or Celeron processor in the 478 pin package.
  - — This design supports the Celeron processor and the Pentium 4 processor (available separately) in the 478 Pin Package. The correct processor voltage is automatically detected by the system board.
  - — The processors have on-board Level 2 cache of 128 Kbytes for the Celeron processor and 512 Kbytes for the Pentium 4 processor. The onboard cache enhances performance for applications requiring high throughput and excellent data handling. This increases performance by lowering memory latencies and making sure the processor does not have to wait for the next data or instruction segment.
- Versatile networking and I/O capabilities:
  - — One Ethernet port
  - — Six USB ports
  - — Two COM ports
  - — Three PCI slots for ease of connectivity to the PCI bus
- 128 Mbytes of DDR266 memory (expandable to 2 GBytes)
- Support for up to four standard IDE hard disk drives

1.1 Content Overview

Chapter 1, "About This Manual" — This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, "Getting Started"— Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, "Theory of Operation" — This chapter provides information on the system design.

Chapter 4, “Hardware Reference”— This chapter provides a description of jumper settings and functions, board debug capabilities, and pinout information for connectors.

Chapter 5, “BIOS Information” — This chapter provides information on the Port 80 values as well as configuring the BIOS for your system. A summary of all BIOS menu options is provided.

Appendix A, “Bill Of Materials” — This appendix contains the bill of materials for the evaluation board.

Appendix B, “Schematics” — This appendix contains schematics for selected connectors and subsystems for the evaluation board.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)
Units of Measure	The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KW	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts

V	volts
mA	microamps, microamperes
mF	microfarads
ms	microseconds
mW	microwatts

Signal Names

Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Support Options

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

Product documentation is provided online in a variety of web-friendly formats at:

http://developer.intel.com/design/litcentr/index.htm

For additional Windows XP Embedded OS information from Microsoft*, please visit:

http://www.microsoft.com/windows/embedded/xp/default.asp

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

Table 1. Related Documents

Document Title	Order Number
Intel® Celeron® Processor on .13 Micron Process in the 478-Pin Package Datasheet	251748
Intel® Celeron® Processor in the 478-Pin Package Specification Update	290749
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 2 GHz - 3.06 GHz Datasheet	298643
Intel® Pentium® 4 processor Specification Update	249199
Intel® Pentium® 4 Processor 478-Pin Socket Design Guidelines	249890
Intel® Pentium® 4 Processor for Embedded Applications Thermal Design Guide	273704
Intel® Pentium® 4 Processor-M for Applied Computing Thermal Design Guide	273729
Intel® 845G/845GL/845GV Chipset Datasheet	290746
Intel® 845G/845GL/845GV Chipset Specification Update	298657
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	290744
Intel® 82801DB I/O Controller Hub 4 (ICH4) Specification Update	290745
Intel® 82802AB/82802AC Firmware Hub (FWH)	290658
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845G/845GL/845GV Chipset Platform Design Guide	298654
Intel® 845G/845GL/845GV Chipset Thermal Design Guide: Intel® 82845G/82845GL/ 82845GV GMCH Thermal and Mechanical Design Guidelines	298655
Intel® 82801DB I/O Controller Hub 4 (ICH4): Thermal and Mechanical Design Guidelines	298651
AP-485 Intel® Processor Identification and the CPUID Instruction	241618
P6 Family of Processors - Hardware Developer's Manual	244001
IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture	245470
The IA-32 Intel® Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	245471
The IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programming Guide	245472
IA-32 Intel® Architecture Software Developer's Manual Documentation Changes	252046
Intel® 82801DB (ICH4), Intel® 82801CA (ICH3), 82801BA (ICH2), 82801AA (ICH), and 82801AB (ICH0) IDE Controller Programmer's Reference Manual	298600
Intel® I/O Controller Hub 4 (ICH4) Enhanced Host Controller Interface (EHCI) Programmer's Reference Manual	298656
Intel® 82802 Firmware Hub Random Number Generator: Programmer's Reference Manual	298029
Design Recommendations for Display Compatibility on Intel® Integrated Graphics Chipsets Application Note	251936
AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions	292276

Getting Started 2

This chapter identifies the evaluation kit's key components, features and specifications. It also tells you how to set up the board for operation.

2.1 Overview

The evaluation board consists of a baseboard (with one Intel® Celeron® processor at 2.0 GHz populated), 845GV chipset, and other system board components and peripheral connectors.

Note: The evaluation board is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals. Since the board is not in a protective chassis, take extra precaution when handling and operating the system.

2.1.1 Baseboard Features

The Intel® 845GV Scalable Performance Board features are summarized below:

CPU

- Supports Intel Celeron processors (2.0 GHz and above) in the 478-pin micro Pin Grid Array (mPGA) package
- Supports Intel® Pentium® 4 Processors in the 478-pin micro Pin Grid Array (mPGA) package
- Supports a 400 MHz and 533 MHz System Bus

Intel 845GV Chipset

- 82845GV Graphics and Memory Controller Hub (GMCH)
- 82801DB I/O Controller Hub 4 (ICH4)
- 82802AC8 Firmware Hub (FWH)
- Supports Ultra ATA 100/66/33 IDE protocol
- Supports integrated graphics based on Intel's Extreme Graphics architecture

Memory Support

- DDR200 and DDR266 system memory interface
- Two 184-pin DIMM slots support DDR SDRAM (unbuffered, non-ECC) modules
- Supports 32-Mbyte to 2-Gbyte using 64 Mbit/128 Mbit/256 Mbit/512 Mbit technology

Flash System BIOS ROM

- AMI system BIOS

Power Supply/Management

- ATX12V* power supply connector

- Heceta 4* Voltage Monitoring system
- Stop clock grant and halt special cycle translation from the host to the hub interface

System I/O

- One floppy connector supporting up to 2.88 Mbytes, and three-mode floppy drives
- Two Ultra ATA* 100/66/33 IDE connectors supporting up to four IDE devices
- Built-in standard/EPP/ECP parallel port connector
- One built-in 16550 fast UART compatible serial port connector
- Six built-in Universal Serial Bus (USB) 2.0 ports
- Built-in PS/2-style keyboard and PS/2 mouse (6-pin mini-DIN) connectors
- One built-in VGA connector
- Built-in integrated network connector
- Built-in audio connectors (Line-in, Line-out, MIC-in) with Yamaha* Audio CODEC
- Built-in audio line-in headers (CD IN and AUX IN)

Peripheral Connectors

- Three PCI expansion slots
- One Communication Network Riser (CNR) slot

Debug Features

- Built-in TAP connector for In-Target Probe
- On-board Port 80 display
- Digital Video Debug port

Miscellaneous Features

- Micro ATX form factor
- Built-in SMBus header
- Built-in standard IrDA TX/RX header
- Built-in Wake On LAN (WOL) header
- Three built-in FAN power connectors (Rear Chassis Fan, CPU Fan, Front Chassis Fan)
- Power/Reset buttons
- Jumper to select FSB clock (100 or 133 MHz)
- Jumper to clear CMOS

2.2 Included Hardware

The following hardware is included in your development kit

- Intel 845GV Scalable Performance Board system platform
- One 2.0 GHz Intel Celeron processor in the 478 pin package
- One fan and heatsink (fansink) thermal solution
- One 128-Mbyte DDR200/266 non-registered DIMM system memory
- Programmed Intel Firmware Hub (N82802AC8)
- Type 2032, socketed 3V Lithium coin cell battery
- Windows XP* Embedded OS compact disc
- Compact disc containing necessary Windows* OS drivers

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The software tools included in your kit are described in this section.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third-party vendors.

2.3.1 AMI BIOS

The Intel® 845GV Scalable Performance Board Development Kit ships pre-installed with AMI BIOS* pre-boot firmware from AMI. AMI BIOS provides an industry-standard BIOS platform to run any standard operating system, including DOS*, Windows* NT, NT Embedded*, Windows 95/98/2000/XP, XP Embedded*, Windows CE*, QNX*, VxWorks*, and Linux* among others. The AMI BIOS Application Kit (available through AMI) includes complete source code, a reference manual, and a Windows-based expert system, BIOStart*, to enable easy and rapid configuration of customized firmware for your Intel 845GV Scalable Performance Board Development Kit.

The following features of AMI BIOS have been enabled in the Intel® 845GV Scalable Performance Board Development Kit:

- DDR SDRAM detection, configuration, and initialization
- Intel® 845GV chipset configuration
- Post codes displayed to port 80H
- Two serial ports, one EPP/ECP parallel port
- PCI bus and device enumeration and configuration

- Integrated video configuration and initialization
- SMC LPC Super I/O programming
- Celeron and Pentium 4 Processor microcode update
- Integrated debugger
- Burn-in diagnostics
- Console redirection
- Manufacturing mode

2.3.2 Windows XP Embedded* (CD Included)

Windows XP Embedded enables rapid development of full-featured connected devices.

Windows XP Embedded is the componentized version of the desktop operating system, enabling rapid development of full-featured connected devices. Based on the same binaries as Windows XP Professional, Windows XP Embedded enables embedded developers to individually select only the features they need for customized, reduced-footprint embedded devices.

Windows XP Embedded with Service Pack 1 also includes componentized features and technologies from Windows XP Professional Service Pack 1. It incorporates the latest embedded-enabling capabilities such as headless support and flexible boot and storage options, such as Remote Boot. In addition, Windows XP Embedded contains the Windows Embedded Studio toolset, which provides access to the componentized Windows technologies and enables developers to rapidly configure, build, and deploy designs.

Information on building a Windows XP Embedded image is not contained within this manual. For a complete step-by-step guide on building the image, please visit Microsoft's Windows XP Embedded support site:

http://www.microsoft.com/windows/Embedded/xp/techinfo/howto/stepguide/default.asp

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

VGA Monitor: You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.

Keyboard: You need a keyboard with a PS/2-style or USB.

Mouse: You need a mouse with a PS/2-style or USB.

Hard Drives, Floppy Drives, and Compact Disk Drives: You can connect up to four IDE drives and two floppy drives to the evaluation board. Two devices (master and slave) can be attached to each IDE connector. A compact disk drive will be required to load the OS. No hard drives or cables are included in your kit; you will need to provide the drives and cables as necessary. You may have all these storage devices attached to the board at the same time.

Video Adapter: You can use the integrated video adapter supplied with your kit, or you can choose to install a PCI video adapter. It is your responsibility to install the correct driver software for any video adapters. Check the BIOS for the proper video settings. See Chapter 5, “BIOS Information” for more information.

Network Adapter: A network interface is populated in the evaluation kit. The network interface will not be operational until after all the necessary drivers have been installed. You may use a different network card other than the interface populated in the kit; you are responsible for installing the correct drivers for such a network card. The evaluation board supports all standard PCI-compatible network cards. You must supply a network cable to connect to the LAN connector or any other network card you chose to install.

Power Supply: You must use an ATX12V power supply with a minimum of 250W support.

Other Devices and Adapters: The evaluation board functions much like a standard desktop computer motherboard. Most PC-compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card.

2.5 Setting Up the Evaluation Board

Once you have gathered the hardware described in Section 2.4, follow the steps below to set up your evaluation board. This manual assumes you are familiar with the basic concepts involved with installing and configuring hardware for a personal computer system.

1. Create a safe work environment.

   Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge damage, and such damage may cause product failure or unpredictable operation.

2. Inspect the contents of your kit.

   Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

Note: The evaluation board is a standard micro-ATX form factor. An ATX chassis may be used if a protected environment is desired.

3. Check the jumper settings.

   J9J1 is used to clear the CMOS memory (pin 2 and 3). Make sure this jumper is set for normal operation (jumper pins 1 and 2). Refer to Section 4.4, “Jumper Functions” on page 34.

4. Check the Front Side Bus (FSB) settings.

   Make sure the FSB and VID jumpers are configured to the correct FSB. Jumper settings are shown in Section 4.4, “Jumper Functions” on page 34.

5. Make sure the following hardware is populated on your evaluation board:

   — One 2.0 GHz Intel Celeron processor

   — One 128-Mbyte DDR SDRAM DIMM (184-pin)

   — One fansink (thermal solution)

6. Install an IDE hard disk drive and CD-ROM drive:

   The evaluation board supports Primary and Secondary IDE interfaces that can each host one or two devices (master/slave). When you are using multiple devices, such as a hard disk and a CD-ROM drive, make sure the hard disk drive has a jumper in the master position and the CD-ROM has a jumper in the slave position. When using a single IDE device with the evaluation board, ensure that the jumpers are set correctly for single drive operation. For jumper settings for different configurations, consult the drive’s documentation. For more information, refer to Section 3.4.6.2.

   — Connect the hard drive’s IDE cable connector to the IDE1 connector on the evaluation board.

   — Connect the other end of the cable to the hard disk drive.

   — Connect a power cable to the hard drive.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the IDE connector header. Connecting the cable backwards can damage the evaluation board or the hard disk.

Note: The Windows XP Embedded CD is only an imaging disk. See Section 2.3.2, "Windows XP Embedded* (CD Included)" on page 14 for additional information on creating the Windows XP Embedded image.

7. Connect any additional storage devices to the evaluation board.
8. Connect a Floppy drive (optional).
   - — Insert a floppy cable into FDC1 (be sure to orient pin 1 correctly).
   - — Connect the other end of the ribbon cable to the floppy drive.
   - — Connect a power cable to the floppy drive.
9. Connect the keyboard and mouse.

   Connect a PS/2-style or USB mouse and keyboard (see Figure 3 on page 33 for connector locations).

Note: U1A1 (on the baseboard) is a stacked PS/2 connector. The bottom connector is for the keyboard and the top is for the mouse.

10. Connect an Ethernet adapter (optional).
11. Connect the audio speakers (optional).

    For audio, connect the audio speakers to the on-board line out connector.
12. Connect the power supply.

    Connect an ATX12 power supply to the evaluation board. Make sure the power supply is not plugged into the wall (turned off). Insert the ATX board connector of the power supply cord into the J2J3 power supply header on the evaluation board. Insert the +12 V power connector of the power supply cord into the J5C1 +12 V header on the evaluation board. After connecting the power supply board connectors, plug the power supply cord into the wall.
13. Power up the board.

    Power and reset are implemented on the evaluation board through buttons located on J9J2 and J8J2, respectively.

    Turn on the power to the monitor and evaluation board. Ensure that the fansink on the processor is operating.

2.6 Configuring the BIOS

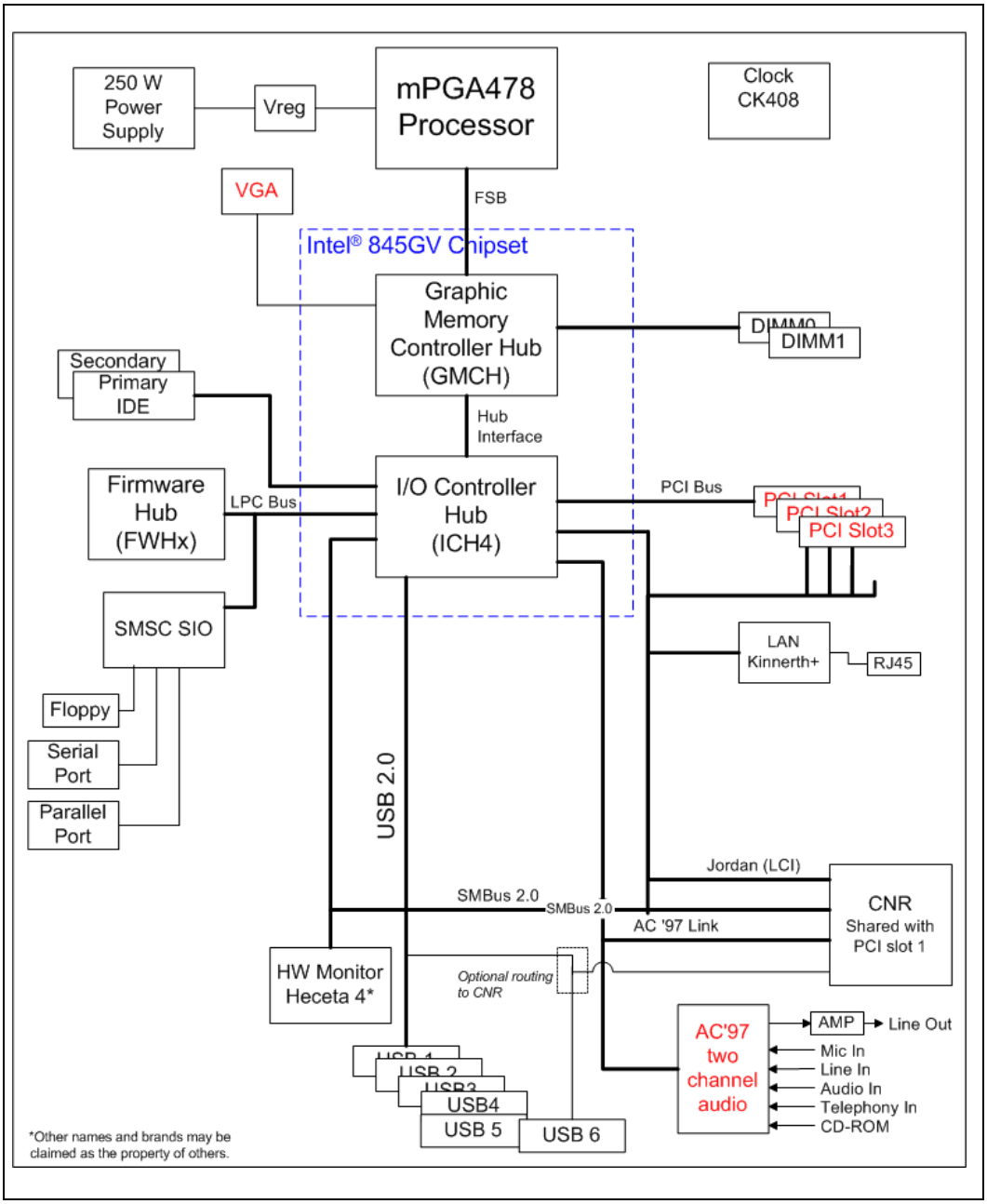
AMI's BIOS is pre-loaded on the evaluation board. You may need to make changes to the BIOS to enable hard disks, floppy disks and other supported features. You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, "BIOS Information" contains a description of BIOS options. BIOS updates may periodically be posted to Intel's Developers' Web site at:

http://developer.intel.com/design/intarch/devkits/

Theory of Operation 3

3.1 Block Diagram

Figure 1. Block Diagram



3.2 Major Features

The following table provides a list of the major features present on the Celeron processor in the 478 Pin Package and 845GV Chipset development kit.

Table 2. Feature Table

Feature	Customer Reference Board Implementation	Comments
Processor	Intel Celeron Processor in the 478 Pin Package	• 400 MHz and 533 MHz System Bus
Chipset	845GV GMCH (Graphic Memory Controller Hub)	• 824 pad footprint (supports both 788 and 760 ball package) • AGTL+ Bus Driver Technology
ICH4	Intel ICH4 (I/O Controller Hub)	• 421 Ball EBGA Package
Memory	DDR SDRAM	• 2 DIMM Slots • Supports up to 512 Mbit Technology (2.5 V) • Supports DDR200 and DDR266 • No ECC Support
Graphics	Integrated Graphics	• Onboard digital debug port
PCI	3 Slots	• 33MHz PCI Bus • PCI Revision 2.2 Specification • PCI Slot 1 can be used for Moon ISA • PCI Slot 2 shares I/O Slot with CNR
LAN	82562EM	• Additional Codecs through CNR
IDE	UltraATA 33/66/100	• 2 Channels, 4 Devices
USB	6 USB Ports	• 2 Front, 3 Back, and 1 through CNR • 2.0 Compatible along with 1.1 support • USB Debug through Port 0
AC'97	Audio Codec	• 2.1 Compliant
Heceta 4	Voltage Monitoring system	• +5 V, +12 V, +3.3 V, +1.5 V, +VCCP, +3.3 VSB
Clock	CK_408	• System Clock
SIO	LPC SMSC X	• Parallel port • Serial port • Floppy controller • Keyboard/Mouse • SMSC LPC47M142–NC (Part Number)
Power Management	S1, S3, S4, S5 States	• ACPI 1.0 Compliant
Debug	TAP Connector For In-Target Probe	• ITP32F Flex Connector
Form Factor	uATX	• Micro ATX Core, board is 9.6" x 9.6"
Power Supply	ATX12V	• 250 W minimum

3.3 Mechanical Diagram

The evaluation board conforms to the micro-ATX form factor. For extra protection in a development environment, you may want to install the evaluation board in an ATX chassis. The evaluation board has three 32 bit/33 MHz PCI connectors, one CNR connector, and two DDR SDRAM DIMM connectors. The system I/O connectors are in the rear of the board.

3.4 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements.

Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with a heatsink/fan thermal solution pre-installed on the processor. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.5 System Operation

The Intel® 845GV Scalable Performance Board Development Kit is designed to support Intel Celeron processors and Intel Pentium 4 Processors in the 478-pin micro Pin Grid Array (mPGA) package. The 845GV chipset includes the GMCH, ICH4, and the FWH.

3.5.1 Intel® Celeron® processor

The Intel Celeron processor on .13 micron process in the 478-pin package expands Intel's processor family into the value-priced PC market segment. Intel Celeron processors provide the value customer the capability to connect to the Internet,and utilize educational programs, home-office software, and productivity applications for an affordable cost. All Celeron processors include an integrated L2 cache, and are built on Intel's advanced CMOS process technology.

- Binary compatible with applications running on previous members of the Intel microprocessor line
- System bus frequency at 400 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advanced Dynamic Execution
  - — Very deep out-of-order execution
  - — Enhanced branch prediction
- 8 KByte Level 1 data cache
- Level 1 Execution Trace Cache stores 12K micro-ops and removes decoder latency from main execution loops
- 128 KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache) with Error Correction Code (ECC)
- 144 Streaming SIMD Extensions 2 (SSE2) Instructions
- Power Management capabilities
  - — System Management mode
  - — Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems

3.5.2 Intel® Pentium® 4 Processor

The Intel Pentium 4 Processor with 512 KB L2 cache on 0.13 micron process is designed for high-performance desktops and entry level workstations. It is binary compatible with previous Intel Architecture processors. The Pentium 4 Processor provides great performance for applications running on operating systems such as Microsoft* Windows 98*, Windows Me*, Windows 2000*, Windows XP*, and UNIX*. This is achieved by the Intel® NetBurst™ microarchitecture, which brings a new level of performance for system buyers. The Pentium 4 Processor extends the power of the Pentium III processor with performance headroom for advanced audio and video internet capabilities. Systems based on Pentium 4 processors also include the latest features to simplify system management and lower the total cost of ownership for large and small business environments.

- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel® NetBurst™ microarchitecture
- System bus frequency at 400 MHz and 533 MHz

- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
  - — Advance Dynamic Execution
  - — Very deep out-of-order execution
- Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12-K micro-ops and removes decoder latency from main execution loops
- 8-KByte Level 1 data cache
- 512-KByte Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - — System Management mode
  - — Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems

3.5.3 Intel® 845GV Chipset

3.5.3.1 Graphics and Memory Controller Hub (GMCH)

The 845GV GMCH provides the processor interface (optimized for Intel® Pentium® 4 Processors and Intel® Celeron® processors), DRAM interface, hub interface and internal graphics. It provides flexibility and scalability in graphics and memory subsystem performance. The following sections describe the reference board's implementation of the 845GV GMCH features.

GMCH features:

- 788-pin FC-BGA package
- 400 and 533 MHz Processor System Bus
- 32-bit host bus addressing
- Eight deep in-order queue
- Processor support
  - — Celeron® processor in a mPGA478 package
  - — Pentium® 4 processor in a mPGA478 package
- System memory controller (DDR implemented)
  - — Two DIMM slots
  - — 200/266 MHz DDR clock
  - — 100/133 MHz SDR clock
- Accelerated hub architecture
- Integrated graphics based on Intel's Extreme Graphics Architecture
  - — Directly supports on-board VGA connector
  - — Supports resolutions up to 2048 x 1536 @ 60 Hz.
- Digital video out port (not implemented)
  - — Operates in single channel and dual channel modes.
  - — Maximum single channel resolution of 1600 x 1200 @ 60 Hz
  - — Maximum dual channel resolution of 2048 x 1536 @ 60 Hz
  - — Supports DVO devices (Flat panel, TV-OUT, etc.)

3.5.3.2 Hub Interface

The 845GV GMCH communicates with the Intel ICH4 via an 8-bit Hub Interface compliant to the Hub Interface Specification Revision 1.5.

3.5.3.3 I/O Controller Hub (ICH4)

The Intel 82801DB I/O Controller Hub (ICH4) is a highly integrated multifunctional I/O controller hub that provides the interface to the PCI bus and integrates many of the functions needed in today's PC platforms. The following sections describe the reference board implementation of the Intel ICH4 features.

ICH4 Features:

- PCI 2.2 with six PCI REQ/GNT pairs
- Eight PCI interrupts
- AC'97 2.2 with seven channel audio support
- LPC interface
- Wake-On-LAN support
- System management
- 24 GPIO signals
- Interrupt controller
- 82C54-based timer
- ACPI 1.0b compliant
- RTC
- 421 BGA package
- Four IDE @ ATA 100 max
- High-speed USB 2.0 host controller supporting all six ports, USB 1.1 compatible
- Enhanced SMBus 2.0 support with slave interface
- Integrated MAC

3.5.3.4 Firmware Hub (FWH)

A socketed 8 Mbit FLASH device is used to store system BIOS and video BIOS, as well as an Intel® Random Number Generator (RNG). A bootblock locking jumper is provided to allow a mechanical means of protecting the bootblock BIOS firmware. All BIOS programming is controlled via software.

FWH Features:

- 32-pin PLCC package
- 8-Mbit flash memory
- Symmetrically-blocked flash memory array (64 Kbyte)
- Pin and register-based block locking
- Integrated hardware RNG
- Single-byte read/write
- Five GPIs

3.5.4 System Memory

3.5.4.1 DDR SDRAM

The customer reference board supports DDR SDRAM main memory. There are two 184-pin DIMM connectors on the board that supports non-registered, non-ECC, single-sided, or double-sided 200/266 MHz DIMMs. These DIMMs provide the ability to use up to 512 Mbit technology for a maximum of 2.0 GByte system memory. The 845GV GMCH provides support only for DDR unbuffered 184-pin DDR SDRAM. The 845GV GMCH does not support double-sided x16 DDR DIMMS.

Caution: Stand-by voltage is applied to the DIMM sockets when the system is in the S3 state. Therefore, do not insert or remove DIMMs unless the system is unplugged.

3.5.4.2 PC133 SDRAM

The 845GV GMCH also supports up to two 168-pin PC133 SDRAM DIMMs, non-registered, single-sided and/or double-sided, up to a maximum of 2.0 GByte system memory. PC133 SDRAM DIMMs are not implemented on the customer reference board.

3.5.5 Boot ROM

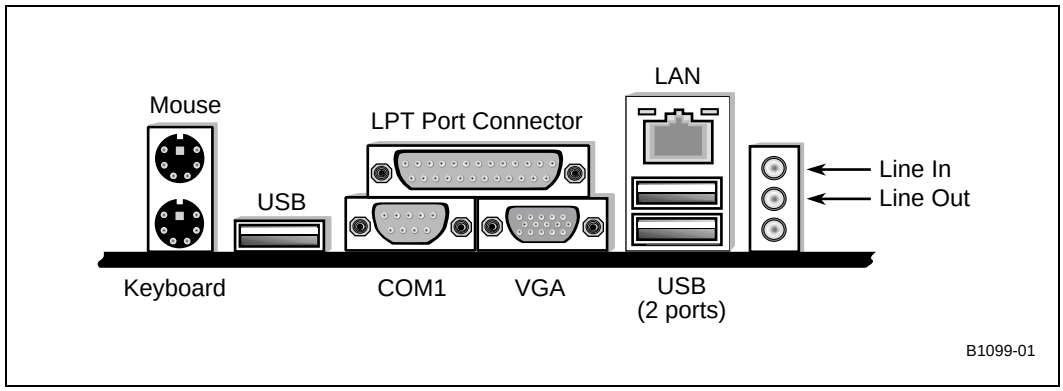
The system boot ROM installed at U9H1 the Intel® FWH, N82802AC8 device. The FWH is socketed and is addressable on the LPC bus off of the ICH4

3.5.6 System I/O

The evaluation board contains the following I/O devices.

- Floppy controller support
- Primary and secondary IDE interface (supports four drives)
- Two serial ports (one on the back panel and one on the front header)
- One parallel port
- Six USB ports (three on the back panel, two on the front header, one through CNR)
- VGA connector
- AC’97 specification compliant audio
- Line Out, Line IN, and MIC IN connectors
- PS/2-style keyboard and mouse ports

Figure 2. Back Panel I/O Connectors



3.5.6.1 PCI-LAN- USB-Audio

The 845GV chipset supports up to six master PCI devices. The board can provide ISA support through the use of jumpers and PCI slot 2 (middle slot). The integrated LAN Connect Interface is routed to either the onboard 82562EM RJ-45 or CNR connector. The six USB 2.0 ports are backward compatible to USB1.1, supporting Hi-Speed, Full-Speed, and Low-Speed devices. Audio has AC'97 2.1 support with three CODECs to support full surround sound (six channel audio) and 20-bit audio.

3.5.6.2 Floppy Disk Drive Support

One 34-pin floppy connector is provided on the evaluation board.

3.5.6.3 IDE Support

The evaluation board supports both a primary and secondary IDE interface via two 40-pin IDE connectors. PRI IDE is the primary interface and SEC IDE is the secondary interface.

There are two IDE channel connectors: primary and secondary. Each channel allows two IDE devices per channel. Supports UltraATA/33/66/100 interfacing.

3.5.6.4 RS-232 Serial Ports

The evaluation board provides one built-in serial port (COM1) and a header for an additional serial port (COM2). COM1 is attached to the back panel I/O connector. COM2 is a header that connects to a serial port cable to provide the additional serial port.

3.5.6.5 IEEE 1284 Parallel Port

One 25-pin DSUB IEEE 1284 parallel port is provided (LPT1).

3.5.6.6 USB Ports

The evaluation board provides three USB connectors on the back panel. Additionally, two USB's are provided in the front headers and one USB is provided through the CNR connector.

3.5.6.7 VGA Connector

This connector is a 15-pin DSUB female connector for output to a monitor.

3.5.6.8 Audio Subsystem

The evaluation board has an integrated (on-board) AC'97 compliant subsystem.

Audio Subsystem Features:

- Line input (back panel)
- Line output (back panel)
- Microphone input (back panel)

3.5.6.9 Keyboard/Mouse

The keyboard and mouse connectors (U1) are PS/2 style, six-pin stacked miniature DSUB connectors. The top connector is for the mouse and the bottom connector is for the keyboard.

3.5.7 Expansion Connectors

The evaluation board contains the following expansion connectors:

- Three PCI 32/33 connectors
- One CNR slot

3.5.7.1 32-bit/33-MHz PCI Connectors

Three industry standard 32-bit/33-MHz PCI connectors (PCI SLOT1, PCI SLOT2, and PCI SLOT3) are provided on the evaluation board.

3.5.7.2 CNR Connectors

One CNR connector is included on the board.

3.5.8 Voltage Monitoring

Heceta 4 provides a voltage monitoring system for fans and voltages of +5 V, +12 V, +3.3 V, +1.5 V, +VCCP, and +3.3 VSB.

3.5.9 Post Code Debugger

An on-board Port 80h display has been implemented on the evaluation board.

3.5.10 Clock Generation

The clock synthesizer on the baseboard generates and distributes the clocks used by the entire system.

The CK_408 generator provides Processor, AGP, GMCH, ICH4, PCI, and USB reference clocks. Clocking for SDRAM is provided by the GMCH.

3.5.10.1 System Clocks

The CK_408 Clock Synthesizer is the primary source of clock generation for most of the clocks on the baseboard. The following clock groups are found on the Intel® 845GV board:

CPU	100 MHz/133 MHz
PCI	33 MHz
SDRAM	100 MHz/133 MHz
3V66	66 MHz (3.3 V)
USB	48 MHz
DOT	48 MHz
REF	14.318 MHz

3.6 Power Management Model

The Intel Pentium 4 Processor in the 478 Pin Package / Northwood Processor and Intel® 845GV Chipset customer reference board supports S1 (Stop Grant), S3 (Suspend to RAM), S4 (Suspend to disk), and S5 (Soft-off) states.

3.6.1 Power Supply Requirements

The Intel® 845GV Scalable Performance Board uses an ATX12V power supply. The 845GV board has a minimum requirement of 250 Watts for proper operation.

3.6.2 Transition to S1 or S3

If enabled, the transition to S1 or S3 from the Full-On state can be accomplished in the following ways:

- The OS will perform the transition through software.
- Pressing the front panel power button for less than four seconds, assuming the OS power management support has been enabled.

3.6.3 Transition to S4

“Wake on S4” (Suspend to disk) is controlled by the Operating System and not the BIOS.

3.6.4 Transition to S5

The transition to S5 is accomplished by the following means:

- Pressing the front panel power button for less than four seconds, if enabled through the OS.

- Pressing the front panel power button for more than four seconds to activate the power button override.

3.6.5 Transition to Full-On

The transition to the Full-On state can be from S1, S3, or S5. The transition from S1 or S3 is a low latency transition that is triggered by one of the following wake events:

- Power management timer expiration
- RTC alarm occurring
- Power button activation
- USB device interrupt
- PME# assertion
- AC'97 link message
- Mouse/Keyboard movement (Applies only to S1 Transition)
- AC Power Loss

For AC power loss, the system operation is defined by register settings in the Intel ICH4. Upon the return of power, a BIOS option, set prior to the power loss, allows the system to either go immediately to the S5 state, or reboot to the Full-On state, no matter what the state prior to the power loss was. External logic for this functionality is not necessary. If the BIOS chooses to remain in the S5 state after AC power loss, only the power button or the RTC alarm can bring the system out of the S5 state. The status of enabled wake events will be lost.

3.7 Battery Requirements

A type 2032, socketed, 3 V lithium coin cell battery is used on this evaluation board.

Hardware Reference 4

This section provides reference information on the hardware, including connector pinout information and jumper settings.

4.1 Thermal Management

The development kit is shipped with a heatsink/fan thermal solution pre-installed on the processor using a clip retention mechanism. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

For additional thermal design information refer to the following documents:

- Intel® Celeron® Processor on .13 Micron Process in the 478-Pin Package Datasheet (order number 251748)
- Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 2 GHz - 3.06 GHz Datasheet (order number 298643)
- Intel® Pentium® 4 Processor for Embedded Applications Thermal Design Guide (order number 273704)
- Intel® 845G/845GL/845GV Chipset Thermal Design Guide (order number 298655)

4.2 Board Debugging

4.2.1 In Target Probe (ITP)

The reference board provides a JTAG-compliant test access port (TAP) for attachment of an In-Target Probe (ITP) with a Flex connector. This port is not the USB Debug Port.

4.2.2 USB Debug Port

A high-speed USB 2.0 Debug port is supported through USB Port 0. This supports the elimination of the legacy COM ports.

4.2.3 Port 80h

The reference board provides a Port 80h display down on the CRB. Please refer to Chapter 5, “BIOS Information” for BIOS POST codes.

4.2.4 Digital Video Debug Port

The Intel® 845GV Scalable Performance Board provides access to all DVO signals via the Digital Video Debug Port.

Table 3. Digital Video Debug Port Connector (J6C1)

DVO Signal Name	Debug Port Pin	DVO Signal Name	Debug Port Pin
DVOB_D0	B63	DVOC_D0	B36
DVOB_D1	A63	DVOC_D1	A36
DVOB_D2	B62	DVOC_D2	B35
DVOB_D3	A62	DVOC_D3	A35
DVOB_D4	B60	DVOC_D4	B33
DVOB_D5	A60	DVOC_D5	A33
DVOB_D6	B57	DVOC_D6	B30
DVOB_D7	A57	DVOC_D7	A30
DVOB_D8	B56	DVOC_D8	B29
DVOB_D9	A56	DVOC_D9	A29
DVOB_D10	B54	DVOC_D10	B27
DVOB_D11	A54	DVOC_D11	A27
DVOB_CLK	B59	DVOC_CLK	B32
DVOB_CLK#	A59	DVOC_CLK#	A32
DVOB_HSYNC	B65	DVOC_HSYNC	B38
DVOB_VSYNC	B65	DVOC_VSYNC	A29
DVOB_BLANK#	B51	DVOC_BLANK#	A38
DVOB_CCLKINT#	A53	DVOBC_INTR#	A26
DVOB_FLDSTL	B53	DVOC_FLDSTL	B26
DVOBC_RCOMP	N/A	ADDID7	A21
MI2CCLK	B41	ADDID6	B21
MI2CDATA	B46	ADDID5	A20
MDVI CLK	A46	ADDID4	B20
MDVI DATA	A41	ADDID3	A17
MDDC CLK	A51	ADDID2	B17
MDDC DATA	A47	ADDID1	A15
		ADDID0	B15

4.2.5 Board Mounted Power Control and Reset Switches

Two switches are provided on the reference board. A power button is connected in parallel to the front panel header pins and to a reset switch. These buttons provide manual power and reset control when the board is not mounted in a chassis.

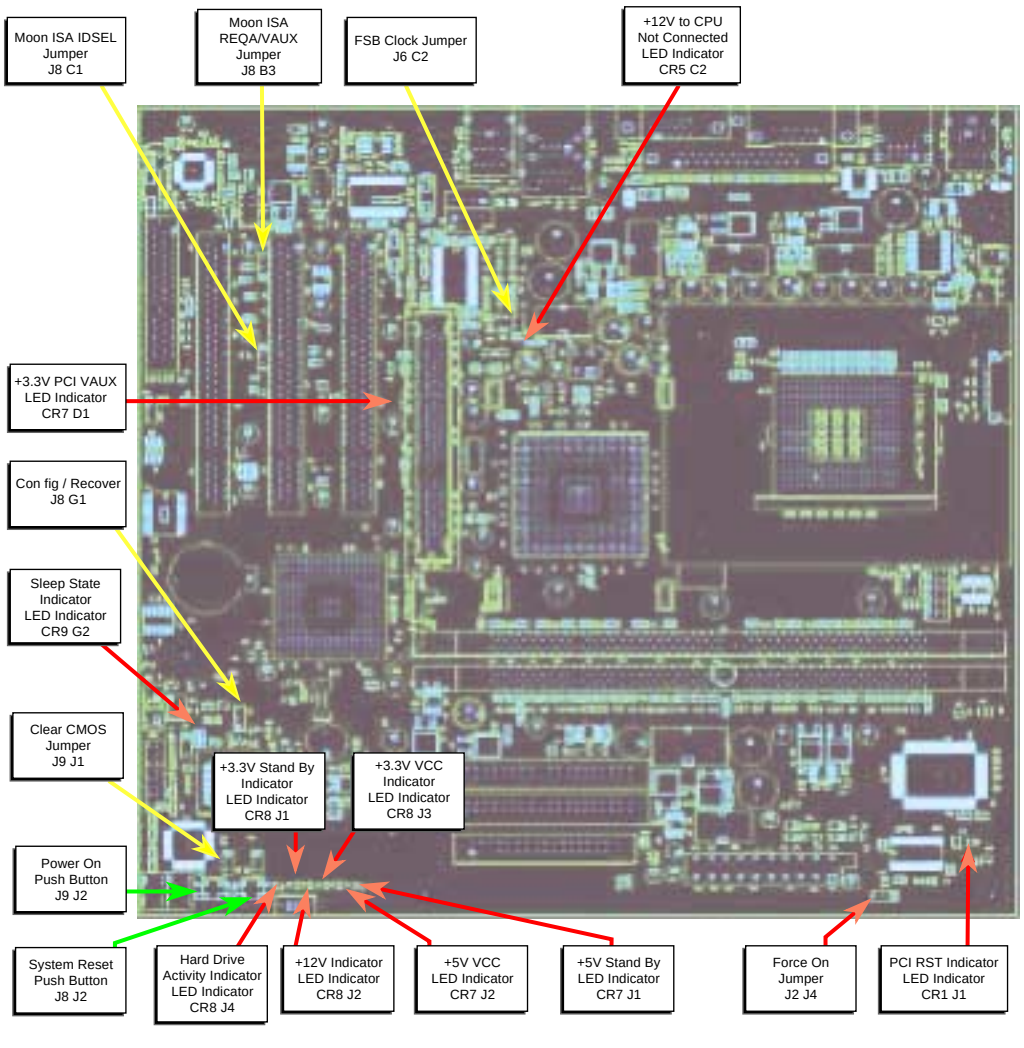
4.2.6 Power LEDs

Power LEDs are on the board to indicate when standby and core power is being applied to the planes. When on, they indicate that no devices should be inserted or removed. Please refer to Section 4.6, “LED Functions” on page 39 for LED function definitions.

Caution: Inserting or removing devices when the Standby Power LEDs are “on” could result in device or board damage.

4.3 Connector Pinouts

Figure 3. Motherboard Layout



4.4 Jumper Functions

Table 4. Jumper Definitions

Reference Designator	Function Description	Settings
J6C2	FSB Clock	• 1-2 CPU SELECT • 2-3 100 MHz x 4 • EMPTY IS 133MHz x 4
J2J4	Power On	• 1-2 Default Setting • 2-3 Force On
J8G1	CONFIG/RECOVER	• 1-2 Normal (Default) • 2-3 Configure • Removed (Recovery)
J8B3	MOON ISA REQA/VAUX	• 1-2 ISA support • 2-3 (Default) no ISA support
J8C1	MOON ISA IDSEL	• 1-2 ISA support • 2-3 (Default) no ISA support
J9D1	AUDIO SDI1/SDI2	• 1-2 • 2-3 (Default)
J1F1 J1F2 J1F3 J1F4 J1F5	VID 4 VID 3 VID 2 VID 1 VID 0	• 2-3 (Default) • 1-2 (Default) • 1-2 (Default) • 1-2 (Default) • 2-3 (Default)
J9J1	Clear CMOS	• 1-2 Normal • 2-3 Clear CMOS
J9J2	Push Button	• Power On
J8J2	Push Button	• System Reset

4.5 Header Functions

Table 5. Header Definitions

Reference Designator	Function Description
J1B1	Rear Chassis Fan
J1D1	ITP Connector
J2F1	CPU Fan
J2A1	Serial Port
J2J3	Standard Power Connector
J6J1	Floppy Connector
J6C1	Digital Video Debug Port
J5C1	+12 V Power Connector
J6G2	Memory – DIMM 1
J6G1	Memory – DIMM 0
J6H1	Secondary IDE Connector
J6H2	Primary IDE Connector
J6B1	AUX IN
J6B2	CD IN
J8B2	PCI Slot 2
J7B1	PCI Slot 1
J6U1	HI LAI HDR
J9B2	PCI Slot 3
J8A2	Audio Front Panel
J8H1	Front Chassis Fan
J8J1	SMBUS HDR
J8B1	AUDIO TELEPHONY
J7H1	USB Front Panel
J9H2	Front Panel Header
J9B1	CNR
J6D2	POC TOOL HDR

4.5.1 ATX12V Power Connector

Table 6. Power Connector (J2J3)

Pin	Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+5 V	+5 V VCC
5	GND	Ground
6	+5 V	+5 V VCC
7	GND	Ground
8	PWRGD	Power Good
9	5 VSB	Standby 5 V
10	+12 V	+12 V
11	3.3 V	3.3 V
12	-12 V	-12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	-5 V	-5 V
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

Table 7. +12V Power Connector (J5C1)

Pin	Name	Function
1	GND	Ground
2	GND	Ground
3	+12 V	+12 V
4	+12 V	+12 V

4.5.2 Enhanced IDE Pinout

Table 8. EIDE Connector Pinout (J6H1 and J6H2)

Pin	Signal	Pin	Signal
1	Reset IDE	21	DRQ3
2	Ground	22	Ground
3	Host Data 7	23	I/O Write
4	Host to Data 8	24	Ground
5	Host Data 6	25	I/O Read
6	Host Data 9	26	Ground
7	Host Data 5	27	I/O Ch Ready
8	Host Data 10	28	Bale
9	Host Data 4	29	DACK 3
10	Host Data 11	30	Ground
11	Host Data 3	31	IRQ 14
12	Host Data 12	32	I/O CS 16
13	Host Data 2	33	Address One
14	Host Data 13	34	Ground
15	Host Data Or 1	35	Address 0
16	Host Data 14	36	Address 2
17	Host Data 0	37	Chip Select 0
18	Host Data 15	38	Chip Select 1
19	Ground	39	Activity
20	Not Used	40	Ground

4.5.2.1 Fan Connectors

Table 9. Fan Connectors

Pin	Signal
1	GND
2	+12 V
3	Not connected

4.5.3 COM Ports

Table 10. COM Ports

COM 1 and COM 2 (DB 9)	
Pin	**Signal**
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.5.4 VGA Adapter Connector

Table 11. VGA Adapter Connector (J1H1)

Pin	Description	Pin	Description	Pin	Description
1	Vid Red	2	Vid Green	3	Vid Blue
4	Not Connected	5	GND	6	GND
7	GND	8	GND	9	5 V Vcc
10	GND	11	Not Connected	12	5 V DDCSDA
13	5 V Hsync	14	5 V Vsync	15	5 V DDCSCL

4.6 LED Functions

Table 12. LED Definitions

Reference Designator	Color	Function
CR5C2	Red	+12 V To CPU Not Connected Indicator
CR7D1	Green	+3.3 V PCI VAUX Indicator
CR9G2	Green/Yellow	Sleep State Indicator
CR8J1	Green	+3.3 V Stand By Indicator
CR7J1	Green	+5 V Stand By
CR1J1	Yellow	PCI RST Indicator
CR8J2	Green	+12 V Indicator
CR8J4	Green	Hard Drive Activity Indicator
CR8J3	Green	+3.3 V VCC Indicator
CR7J2	Green	+5 V VCC Indicator
DS9J1	Red	7 Segment Display (POST Code)
DS9J2	Red	7 Segment Display (POST Code)

This page intentionally left blank.

BIOS Information 5

Please refer to the documentation/CD included in the kit for third party BIOS references.

For AMI BIOS Post codes, please visit: http://www.ami.com

This page intentionally left blank.

Bill Of Materials A

Table 13. Bill of Materials for Intel Manufactured Parts

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
29	1	U6D1	BDG_DDR_2P0_FCBGA	INTEL CORP	RG88BKG QD14
84	1	U9H1	FWH_4M_PLCC	INTEL CORP	N82802AB SB48
91	1	U8F1	ICH4_BGA	INTEL CORP	FW82801DB QC66
101	1	U7A2	KINNERETHPLUS_SSOP	INTEL CORP	DA 82562 EM SL4KN

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 1 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
1	2	J9G1,J9G3	CONN,HDR,1 X 2,PLG,VT,0.1,093 ST,KP PG >	FOXCONN ELECTRONICS, INC.*	HF06021-P1
2	7	J2J1,J2J2,J3J1,J3J2,J8A1,J8H2,J8H3	1X2HDR_TH	WIESON ELECTRONIC*	2100C888-051
3	1	J9H1	1X3HDR2_TH	WIESON ELECTRONIC	2100C888-002
4	14	J1F1-J1F5,J2J4,J6C2,J7D1,J8B3,J8C1,J8G1,J8J1,J9D1,J9J1	1X3HDR_TH	WIESON ELECTRONIC	2100C888-001
5	3	J1B1,J2F1,J8H1	1X3HDR_TH1MT	FOXCONN ELECTRONICS, INC.	HF08030-P1
6	1	J6B1	1X4HDR_COLOR_TH	TYCO ELECTRONICS CORPORATION*	147050-1
7	1	J8B1	1X4HDR_COLOR_TH	TYCO ELECTRONICS CORPORATION	147050-2
8	1	J6B2	1X4HDR_TH1MT	TYCO ELECTRONICS CORPORATION	104450-3
9	1	J2J3	2X10PWR_1MH	FOXCONN ELECTRONICS, INC.	HM25100-P1
10	1	J6J1	2X17HDR3_5_TH	TYCO ELECTRONICS CORPORATION	1364552-1
11	1	J6H1	2X20HDR20_TH	WIESON ELECTRONIC	2120C888-005
12	1	J6H2	2X20HDR20_TH	WIESON ELECTRONIC	2120C888-002
13	1	J6U1	2X25X2MGT_SM	ROBINSON NUGENT	P08-050SL-A-G
14	1	J5C1	2X2HDR_1MH	FOXCONN ELECTRONICS, INC.	HM25020-P1
15	1	J9G2	2X3HDR2_TH	WIESON ELECTRONIC	2100C888-062
16	1	J9H3	2X3HDR4_TH	WIESON ELECTRONIC	2100C888-026
17	1	J9H2	2X5HDR10_TH	WIESON ELECTRONIC	2100C888-003

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 2 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
18	1	J8A2	2X5HDR8_TH	WIESON ELECTRONIC	2100C888-042
19	1	J7H1	2X5HDR9_TH	WIESON ELECTRONIC	2100C888-045
20	3	U1J1,U6C1,U6C2	74AHCT1G08_SM	TEXAS INSTRUMENTS*	SN74AHCT1G08 DBVR
21	1	U9F1	74LVC00A_SM	PHILIPS COMPONENTS	74LVC00AD
22	1	U8B1	78M05C_SOT369	NATIONAL SEMICONDUCTOR	LM78M05CDT
23	1	U9A1	AD1981_PQFP	ANALOG DEVICES	AD1981JST
24	1	RM6C1	AGP_RM_CLIP	FOXCONN ELECTRONICS, INC.	006-0002-939
25	4	J4D1,J4F1,J6D1,J6F1	ANCHOR_CLP_GHST	FOXCONN ELECTRONICS, INC.	HB96030-DW
26	1	U9D1	AT93C46A_66_SOIC	ATMEL	AT93C46-10SI-2.7
27	1	J6A1	AUDIO3STACK_TH	FOXCONN ELECTRONICS, INC.	JA33331-G05
28	1	BT8F1	BATT_HLDR_2PIN_TH	CHIA TSE TERMINAL INDUSTRY CO., LTD.*	B6615BP5Q
30	1	C7G6	CAP-P_7343		
31	68	C1A4,C2B1,C2B10-C2B13,C2F1,C2G18,C2G19,C2J5,C3B4-C3B6,C3G16,C3H1,C3H3,C3H8,C3H9,C4B4-C4B6,C4C1-C4C5,C4F2,C4H1,C4J4,C4J6,C4J7,C5A6,C5B7,C5B10,C5C2,C5C3,C5C6,C5C7,C5F8,C5G19,C6C8,C6C11,C6D1,C6D3,C6E2,C6E11,C6F1,C6G4,C6G11,C7C10,C7D6,C7E3,C7G2,C7G5,C7H2,C8A1,C8A4,C8B1,C8B9,C8B10,C8C2,C8C5,C8D4,C8D5,C8E3,C8E4,C8G4,C9A1	CAP-P_RDL		
32	17	C1B4-C1B6,C2A9,C3A13,C3H5,C3H7,C5B8,C5D8,C6B2,C6B3,C6C1,C6C6,C6D4,C7A11,C7A13,C7B7	CAPN_1206	TDK CORPORATION OF AMERICA*	C3216Y5V1C475 ZT0K9N
33	7	C1G1,C3G3,C5F7,C5G21,C5H1,C6G10,C7H1	CAPN_1206	TDK CORPORATION OF AMERICA	C3216X5R1A475 KT009N
34	18	C2C1-C2C9,C3C2-C3C4,C3C8,C3C9,C5D4,C5D5,C6H1,C9C4	CAPN_1206	TDK CORPORATION OF AMERICA	C3216X7R0J106 MT0S9N
35	2	C3C1,C3C11	CAPN_1210	TDK CORPORATION OF AMERICA	C3225X5R0J226 MT009N

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 3 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
36	6	C1,C6C5,C7A15,C7J2,C8B11,C8H7	CAPN_603	MURATA ELEC. NORTH AMERICA*	GRM39X7R102K050AJ
37	217	C1A8,C1B1,C1C1,C1C3,C1C4,C1F1,C1F3,C1F4,C1G3,C1H1-C1H4,C1J1,C1J3,C2G1-C2G3,C2G5-C2G17,C2H2,C2H3,C2J1-C2J4,C2J6,C3F1,C3G1,C3G2,C3G4-C3G15,C3H6,C3J1,C3J3,C3J5-C3J7,C4A16,C4G1-C4G14,C4J2,C4J3,C4J8,C5B1,C5B6,C5D3,C5G1-C5G18,C5J1,C6B1,C6C9,C6C10,C6C12,C6C13,C6D2,C6E5,C6E12,C6F3,C6G2,C6G3,C6G5-C6G9,C6G12,C6G13,C6H2,C7A9,C7A10,C7A12,C7A14,C7A16,C7A17,C7B3-C7B6,C7B8,C7B17,C7B22,C7C4,C7C8,C7C9,C7D1-C7D5,C7D7-C7D10,C7E1,C7E2,C7E4-C7E8,C7F4,C7F5,C7F7,C7F9,C7F10,C7G1,C7G3,C7G4,C7J1,C8B7,C8B8,C8C1,C8C3,C8C4,C8D1-C8D3,C8D6,C8D7,C8E1,C8E2,C8E5-C8E7,C8F1-C8F3,C8G1-C8G3,C8G11,C8G12,C8H1-C8H3,C8H5,C8H6,C9B6-C9B8,C9C1-C9C3,C9C5-C9C8,C9D1-C9D5,C9E1-C9E4,C9F1-C9F3,C9G1,C9G3,C9G4,C9G6-C9G9,C9U1	CAPN_603	TDK CORPORATION OF AMERICA	C1608Y5V1E104ZT009N
38	6	C1B2,C2B4-C2B8	CAPN_603	KEMET	C0603C223K5RAC9045
39	12	C1C2,C1H5,C3C5,C3C6,C3H2,C5H2,C6B10,C7J3,C8G5,C8G9,C9E5,C9H4	CAPN_603	TDK CORPORATION OF AMERICA	C1608Y5V1A105ZT009N

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 4 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
40	72	C1C5,C1C6,C1F2,C2B9,C2G4,C2H1,C3C7,C3H4,C4D1,C4D2,C4E1-C4E3,C4F1,C4H3,C4H4,C5D1,C5D6,C5D7,C5D9,C5D11-C5D20,C5F1-C5F6,C5G20,C5H3,C6B4-C6B6,C6B9,C6C3,C6C7,C6D5-C6D7,C6E1,C6E3,C6E4,C6E6,C6E7,C6E10,C6E13,C6F2,C6F4-C6F6,C6G1,C6G14,C7B14,C7B16,C7B21,C7B25,C7C7,C7F2,C7F3,C8G7,C9H6,C9J1-C9J3	CAPN_603	TDK CORPORATION OF AMERICA	C1608X7R1C104KT009T
41	1	C1G2	CAPN_603	MURATA ELEC. NORTH AMERICA	GRM39X7R101K050AJ
42	2	C1J2,C9G2	CAPN_603	TDK CORPORATION OF AMERICA	C1608C0G1H470JT009A
43	1	C2B2	CAPN_603	TDK CORPORATION OF AMERICA	C1608X7R1C683KT009N
44	5	C3B1,C4B1,C4H2,C5B11,C5B12	CAPN_603	MURATA ELEC. NORTH AMERICA	GRM39X7R472M050AJ
45	1	C3C10	CAPN_603	KEMET*	C0603C221K5RAC9045
46	16	C3J2,C3J4,C4J9,C5B2-C5B5,C5C4,C5C5,C7B12,C7C11,C7H3,C7H4,C9G5,C9H1,C9H2	CAPN_603	KEMET	C0603C471K5RAC9045
47	8	C4J1,C5D2,C5D10,C6E8,C6E9,C7F1,C7F6,C7F8	CAPN_603	MURATA ELEC. NORTH AMERICA	GRM39X7R103K050AJ
48	1	C6A8	CAPN_603	TDK CORPORATION OF AMERICA	C1608C0G1H8R2CT009A
49	21	C6B7,C6B8,C6C2,C6C4,C7B9-C7B11,C7B13,C7B15,C7B18-C7B20,C7B23,C7B24,C7C1-C7C3,C7C5,C7C6,C8G8,C8G10	CAPN_603	TDK CORPORATION OF AMERICA	C1608C0G1H100DT009A
50	2	C7B1,C7B2	CAPN_603	TDK CORPORATION OF AMERICA	C1608C0G1H330JT009A
51	3	C8G6,C9H3,C9H5	CAPN_603	TDK CORPORATION OF AMERICA	C1608X7R1C473KT009N
52	4	C1B3,C3B2,C4B2,C5B9	CAPN_805	MURATA ELEC. NORTH AMERICA	GRM40X7R105K016AK
53	1	C2B3	CAPN_805	TDK CORPORATION OF AMERICA	C2012X7R1C224KT009N
54	24	C2D1-C2D18,C2E1-C2E4,C3E1,C3E2	CAPN_805	AVX CERAMICS CORP	08056D106MAT4A

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 5 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
55	3	C3B3,C4B3,C5C1	CAPN_805	TDK CORPORATION OF AMERICA	C2012Y5V1C225 ZT0S9N
56	1	C4J5	CAPN_805	TDK CORPORATION OF AMERICA	C2012Y5V1C105 ZT009N
57	1	U6B1	CK_408_SSOP	CYPRESS ELECTRONICS*	W320-04H
58	1	J9B1	CNR60_ICH4_TH	FOXCONN ELECTRONICS, INC.	EH03011-GU-N
59	1	J2A2	CON2XUSB_TH	FOXCONN ELECTRONICS, INC.	UB11123-5D1
60	1	J1	CONAGP1_5V	FOXCONN ELECTRONICS, INC.	EE06250
61	3	J7B1,J8B2,J9B2	CONPCI2_2_TH	FOXCONN ELECTRONICS, INC.	EH06011-GL-1
62	3	CP4A1,CP9H1,CP9H2	CPAK4C4C_SM		
63	1	Y7A1	CRYSTAL_SM	RALTRON*	630770-011
64	1	Y7B1	CRYSTAL_SM	CITIZEN AMERICA CORP.*	HCM4914.31818 MBBKT
65	1	Y9A1	CRYSTAL_SM	CITIZEN AMERICA CORP.	HCM4924.576MB BJTR
66	1	U2B1	CS5323_SOIC	ON SEMICONDUCTOR*	CS5323GDWR20
67	3	TPA3H1,TPA4H1,TPA6G1	DEBUG_PAD_TP		
68	2	J6G1,J6G2	DIMM2P_184_CK_TH	FOXCONN ELECTRONICS, INC.	AT09217-P1
69	8	CR2A1-CR2A4,CR6A1-CR6A4	DIODE_DUAL_SM	LITTELFUSE INC*	PGB0010603NR
70	2	CR2H1,CR8G1	DIOSOT23C_SOT23C	I T T SEMICONDUCTOR*	BAT54C
71	6	CR5D1-CR5D3,CR6C1,CR6C2,CR9B1	DIOSOT23S_SOT23S	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC*	MMBD7000LT1
72	2	CR9F1,CR9G1	DIOSOT23S_SOT23S	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC	BAV99LT1
73	1	J4A1	DSUB15_TH-2MT	FOXCONN ELECTRONICS, INC.	DZ11A31-5P9
74	1	J4A2	DSUB25TALL_TH-3MT	FOXCONN ELECTRONICS, INC.	DM11351-PR1
75	1	J2A1	DSUB9_TH-2MT	FOXCONN ELECTRONICS, INC.	DT10121-PR9
76	1	CR9G2	DUAL_LED_ALT	STANLEY ELECTRIC SALES OF AMERICA*	AYPG1204W-170-TR
77	1	U9J1	EPM7032_PQFP	ARROW ELECTRONICS*	EPM7032AETC44-10
78	1	FB1A2	FERRITE_SM	MURATA ELEC. NORTH AMERICA	BLM21P300SPT1
79	2	FB6B1,FB6C1	FERRITE_SM	KOA SPEER ELECTRONICS*	MCB1206FTED301P

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 6 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
80	1	Q2F1	FET_SOT23	SILICONIX*	SI2302DS-T1
81	6	Q6B1,Q7E1,Q8D2,Q8H1,Q9G2,Q9G3	FET_SOT23	DIODES INC/LITEON POWER SEMI*	BS870
82	5	Q2B1,Q4B1,Q5B1,Q6G1,Q6H1	FET_VREG_SOT	ON SEMICONDUCTOR	NTD4302T4
83	9	Q3B1-Q3B3,Q4B2-Q4B5,Q4C1,Q4C2	FET_VREG_TH	ST MICROELECTRONICS*	D40NF3LL-1(034Y)
85	1	U2A1	GD75232S_SSOP		
86	1	U2J1	GLUECHIP4_SSOP	PHILLIPS SEMICONDUCTORS	PCA9504A
87	1	JDR2P1	GND_ISOLATION_SM		
88	1	U1F2	HECETA4_SSOP	ANALOG DEVICES*	ADM1025ARQ-REEL
89	1	U1F1	HECETA6_SSOP	ANALOG DEVICES	ADM1027XRQ-0REEL
90	3	U3B1,U4B1,U5B1	HIP6601_SOIC	INTERSIL CORPORATION	HIP6601CB-T
92	3	L3C1,L3C2,L6D1	INDUCTOR_SM	TDK CORPORATION OF AMERICA	MLZ2012E100PTA1N
93	1	L5D1	INDUCTOR_SM	TDK CORPORATION OF AMERICA	MLF1608DR82KTA1N
94	1	L5F1	INDUCTOR_SM	TDK CORPORATION OF AMERICA	MLF2012DR68KTA1N
95	1	L6E1	INDUCTOR_SM	TDK CORPORATION OF AMERICA	NLFC322522T-1R0M
96	1	L7A1	INDUCTOR_SM	MURATA ELEC. NORTH AMERICA	LQG21N4R7K10T2
97	3	L2B1,L3B1,L4B1	INDUCTOR_TH	BI TECHNOLOGIES	HM00-99696
98	2	L3J1,L5C1	INDUCTOR_TH	BI TECHNOLOGIES	HM00-99521
99	1	L4H1	INDUCTOR_TH	PULSE ENGINEERING	PA0125
100	4	L2A1,L2A2,L6B1,L6B2	IND_4PIN_ACM2012	TDK CORPORATION OF AMERICA	ACM2012-900-2P-TL
102	1	LB5J1	LABEL_SILK		
103	1	LB3J1	LABEL_SM	BRADY CORPORATION*	056145
104	2	DS9J1,DS9J2	LED_DISPLAY_10P_DS	STANLEY ELECTRIC SALES OF AMERICA*	NAR131S-C
105	2	CR1J1,CR7D2	LED_SM	STANLEY ELECTRIC SALES OF AMERICA	AA1112H-TR
106	1	CR5C2	LED_SM	STANLEY ELECTRIC SALES OF AMERICA	BR1102W
107	7	CR7D1,CR7J1,CR7J2,CR8J1-CR8J4	LED_SM	STANLEY ELECTRIC SALES OF AMERICA	PG1112H-TR
108	1	U7A1	LF353_SOI8	NATIONAL SEMICONDUCTOR	LF353MX
109	1	U1E1	LM317L_SOIC	NATIONAL SEMICONDUCTOR	LM317LMX

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 7 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
110	1	U2H1	LM358_SOIC	NATIONAL SEMICONDUCTOR	LM358MX
111	1	U8A1	LM4871_SOIC	NATIONAL SEMICONDUCTOR	LM4871
112	1	LB3F1	LOGO_SILK		
113	1	U1H1	LPC47M102_PQFP	STANDARD MICROSYSTEMS CORP.	LPC47M102S-MC
114	6	Q1B1,Q7H1,Q8C1,Q8D1,Q8H4,Q9B1	MBT3904DUAL_SOT	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC	MBT3904DW1T1
115	1	U7J2	MC33269_SOT369	NATIONAL SEMI-CONDUCTOR, INC.	LM1117DTX-ADJ
116	1	U7G1	MC33567_SM	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC	MC33567D-1R2
117	1	J8J3	MFG_MODE_JMPR_SM		
118	1	U1C1	MIC5248_SOT	MICREL INC*	SPN020060
119	1	U5H2	MIC5255_SOT	MICREL INC	MIC5255-2.5BM5
120	1	J1D1	MINI_ITP_28P	MOLEX CONNECTOR CORPORATION*	524352891
121	1	Q3G1	MTD3302_SOT	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC	MTD3302T4
122	1	C9A34	NCAP_1206	TDK CORPORATION OF AMERICA	C3216Y5V1C475ZT0K9N
123	3	C6A2,C6A3,C9A7	NCAP_402	AVX CERAMICS CORP*	04025C471KAT4A
124	4	C6A4-C6A7	NCAP_402	TDK CORPORATION OF AMERICA	C1005X7R1H221KT009A
125	1	C7A2	NCAP_402	TDK CORPORATION OF AMERICA	C1005C0G1H470JT009A
126	12	C7A3,C7A8,C8B4,C8B5,C9A12,C9A14,C9A17,C9A20,C9A25,C9A31,C9A32,C9A35	NCAP_402	TDK CORPORATION OF AMERICA	C1005Y5V1C104ZT009N
127	1	C9A16	NCAP_402	AVX CERAMICS CORP	0402YC473KAT4A
128	2	C9A2,C9A6	NCAP_402	TDK CORPORATION OF AMERICA	C1005X5R1A104KT009N
129	2	C9A33,C9B2	NCAP_402	TDK CORPORATION OF AMERICA	C1005C0G1H220JT009A
130	1	C9A8	NCAP_402	TDK CORPORATION OF AMERICA	C1005X7R1E472KT
131	1	C9B1	NCAP_402	TDK CORPORATION OF AMERICA	C1005C0G1H100DT009A
132	1	C9B5	NCAP_402	AVX CERAMICS CORP	04025A5R6DAT4A

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 8 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
133	15	C1A1,C1A3,C1A5-C1A7,C2A1,C2A4-C2A7,C3A8-C3A11,C5A1	NCAP_603	KEMET	C0603C471K5RAC9045
134	8	C1A2,C9A19,C9A22,C9A26-C9A30	NCAP_603	TDK CORPORATION OF AMERICA	C1608X5R0J105MT009N
135	4	C2A2,C2A3,C2A8,C4A15	NCAP_603	TDK CORPORATION OF AMERICA	C1608Y5V1E104ZT009N
136	17	C3A1-C3A7,C3A12,C4A6-C4A14	NCAP_603	KEMET	C0603C221K5RAC9045
137	6	C4A1-C4A4,C5A3,C5A5	NCAP_603	KEMET	C0603C339C5GAC9045
138	3	C4A5,C5A2,C5A4	NCAP_603	KEMET	C0603C229C5GAC9045
139	18	C6A1,C7A1,C7A4,C7A5,C7A7,C8A2,C8A3,C8A5-C8A8,C8B3,C8B6,C9A13,C9A18,C9A21,C9A23,C9A24	NCAP_603	TDK CORPORATION OF AMERICA	C1608Y5V1A105ZT009N
140	1	C7A6	NCAP_603	TDK CORPORATION OF AMERICA	C1608C0G1H100DT009A
141	4	C9A3,C9A4,C9A10,C9A11	NCAP_603	AVX CERAMICS CORP	06035A271JAT$A
142	1	C9B4	NCAP_603	KEMET	C0603C223K5RAC9045
143	1	C8B2	NCAP_805	TDK CORPORATION OF AMERICA	C2012Y5V1C105ZT009N
144	2	C9A5,C9A15	NCAP_805	AVX CERAMICS CORP*	08056D106MAT4A
145	1	C9A9	NCAP_805	TDK CORPORATION OF AMERICA	C2012X5R1A105KT0S9N
146	1	C9B3	NCAP_805	TDK CORPORATION OF AMERICA	C2012Y5V1C225ZT0S9N
147	6	FB6A1-FB6A6	NFERRBD_SM	TDK CORPORATION OF AMERICA	MMZ1608Y601BTA1N
148	4	FB1A1,FB1A3-FB1A5	NFERR_SM	TDK CORPORATION OF AMERICA	MMZ1608Y601BTA1N
149	3	FB4A1,FB5A1,FB5A2	NFERR_SM	MURATA ELEC. NORTH AMERICA	BLM18BB750SN1D
150	1	L8B1	NIND_SM	TDK CORPORATION OF AMERICA	NL322522TL-R27J
151	12	Q1,Q1B2,Q1G1,Q1G2,Q1J1,Q2J1,Q3H1,Q3J1,Q5C1,Q6C1,Q7C1,Q7D1	NPN_SOT23	PHILIPS COMPONENTS	PMBT3904
152	2	Q1B3,Q8H2	NPN_SOT23	PHILIPS COMPONENTS	PMBT2222A T/R
153	1	R8B3	NRES_1206	ROHM CORPORATION*	MCR18EZHJ000

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 9 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
154	35	R3R1,R5R1,R6A2,R7A8,R7A9,R7A20,R7A21,R7A28,R7U1,R8B1,R8B2,R9A1,R9A2,R9A6-R9A14,R9A17,R9A18,R9A23,R9A24,R9B2-R9B5,R9B13-R9B17	NRES_402	KOA SPEER ELECTRONICS*	RM73Z1ET
155	7	R7A1,R7A3,R7A23,R7A25,R9A5,R9A22,R9B9	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP103J
156	6	R7A10,R7A19,R7A33,R9B1,R9B7,R9B8	NRES_402	AVX CERAMICS CORP	CR05-222J-H
157	4	R7A5,R7A11,R7A18,R7A26	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP100J
158	3	R7A12,R9A15,R9A16	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP102J
159	1	R7A13	NRES_402	KOA SPEER ELECTRONICS	RK73H1ETP1100F
160	2	R7A2,R7A14	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP471J
161	1	R7A15	NRES_402	AVX CERAMICS CORP	CR05-3010F-H
162	1	R7A16	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP221J
163	1	R7A17	NRES_402	AVX CERAMICS CORP	CR05-2490F-H
164	4	R7A6,R7A22,R7A27,R8A5	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP472J
165	1	R7A24	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP223J
166	1	R7A4	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP104J
167	1	R7A7	NRES_402	VISHAY- DALE ELECTRONICS INC*	CRCW0402122JRT7
168	3	R8A1-R8A3	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP203J
169	3	R8A4,R8A6,R9B6	NRES_402	AVX CERAMICS CORP	CR05-1001F-H
170	1	R9A19	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP101J
171	2	R9A20,R9A21	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP330J
172	2	R9A3,R9A4	NRES_402	VISHAY- DALE ELECTRONICS INC	CRCW0402334JRT7
173	2	R9B10,R9B12	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP473J
174	1	R9B11	NRES_402	KOA SPEER ELECTRONICS	RM73B1ETP202J
175	7	R1C9,R1C10,R6A1,R6C17,R6C18,R6C22,R9H8	NRES_603	ROHM CORPORATION	MCR03EZHJ000
176	3	R4A1,R5A3,R5A5	NRES_603	PANASONIC INDUSTRIAL*	ERJ3EKF75R0Z
177	3	R4A2,R5A2,R5A4	NRES_603	VISHAY- DALE ELECTRONICS INC	CRCW060337R4FRT5
178	1	R4A3	NRES_603	KOA SPEER ELECTRONICS	RM73B1JTDD103J
179	4	R5J1-R5J4	NRES_603	KOA SPEER ELECTRONICS	RM73B1JTDD101J
180	1	R4A4	NRES_805	ROHM CORPORATION	MCR10EZHMJ000

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 10 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
181	1	J2E1	NWD478_GB_SKT	FOXCONN ELECTRONICS, INC.	PZ47807-2748-01
182	2	Q4H1,Q4H2	PHD55N03LT_SOT	PHILIPS SEMICONDUCTORS	PHD55N03LT
183	1	Q2G1	PMOSFET_DPAK	STMICROELECTRONICS	STD10PF06
184	1	Q9G1	PNP_SOT23	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC	MMBT3906
185	1	J6D2	POCTOOL_CONN_SM	MOLEX CONNECTOR CORPORATION	79109-8004
186	1	J1A1	PS2STACK_TH	FOXCONN ELECTRONICS, INC.	MH11061-PD5
187	1	Q1C1	PZT2222A_SM	PHILIPS COMPONENTS	PZT2222A
188	42	R1,R1B5,R1C6,R1F3,R1F11-R1F15,R1G3,R1J5,R2B3,R2B10,R2G3,R2H2,R3R2-R3R5,R4J1,R6B27,R6B29,R6C3,R6C5,R6C14,R6C15,R6E2,R6E3,R6G2,R6G3,R6G5,R6H1,R7D1,R7H6,R7H8,R8G11,R8G13,R8H4,R8H14,R8H15,R8J5,R9H2	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD102J
189	2	R1A1,R8H17	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD154J
190	50	R1B1,R1B6,R1B9,R1C3,R1F1,R1F2,R1J4,R2J3,R5A1,R5B1,R6B22,R6C9,R6G4,R7B1,R7D5,R7F1-R7F8,R7F16,R7H2,R7H4,R7H7,R8E1,R8G2-R8G4,R8G6,R8G8,R8H8,R8H11,R9C1-R9C5,R9D1,R9D8,R9F5,R9G4,R9G7-R9G9,R9H4,R9H5,R9H7	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD103J
191	4	R1B10,R6C4,R9G11,R9G14	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD152J
192	5	R1B11,R2F3,R8H6,R9H9,R9H11	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD153J
193	22	R1B12,R1H2,R1H3,R1H5,R1H7,R2B9,R2F2,R2H7,R2J2,R3H11,R3J1,R3J3,R4D2,R6E5,R7D3,R7G6,R7G11,R8G5,R8H5,R8H13,R8J2,R9G1	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD472J
194	1	R1B2	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD5622

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 11 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
195	98	R1B3,R1B8,R1C4,R1C7,R1F4-R1F10,R1G2,R1H1,R1H8,R1J3,R2A1-R2A4,R2F1,R2F4,R2F6,R2G4,R2H3-R2H6,R2H10,R2H11,R3C3,R3H3,R3H4,R3H6,R3H7,R3H9,R3J2,R4D1,R4H2,R5B2,R5B3,R5D5,R5T1,R6B1-R6B4,R6B7,R6B9,R6B15,R6C7,R6C8,R6C10,R6C13,R6F1,R6F6,R6N1,R7B3,R7C1,R7E6,R7F12,R7F14,R7F15,R7F17,R7F18,R7G3,R7G4,R7G9,R7G10,R7H1,R7H3,R7H5,R7T1,R7T2,R8C1-R8C6,R8E2,R8F1,R8H1,R8H7,R8H16,R8J1,R8J3,R8J8,R9C6,R9C7,R9D2,R9F1-R9F4,R9F6,R9G2,R9G5,R9G6	RESN_603	ROHM CORPORATION	MCR03EZHJ000
196	22	R1C1,R2F7-R2F10,R2H1,R3F1-R3F4,R3H5,R4F1,R4F2,R5F2-R5F5,R6C2,R6F7,R6F8,R7G8,R8H3	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD100J
197	1	R1C2	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD242J
198	2	R1C5,R2G5	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD151J
199	2	R1D1,R5D3	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031500FRT5
200	2	R1D2,R3D1	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD510J
201	1	R1D3	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD750J
202	1	R1D4	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD270J
203	1	R1D5	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD681J
204	1	R1D6	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD390J
205	2	R1D7,R3D3	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD51R1F
206	11	R1G1,R2C1,R5H1,R6C11,R7D2,R7D4,R8J4,R8J6,R8J9,R9H1,R9H3	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD221J
207	2	R1H4,R1H6	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD471J
208	6	R1J1,R1J2,R7E5,R7J1,R8J7,R9H12	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD331J

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 12 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
209	8	R1J6,R1J7,R3H8,R5C2,R8C7,R8D1,R9E1,R9G10	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD272J
210	2	R2B1,R7E9	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD20R0F
211	1	R2B2	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06035761FRT5
212	1	R2B4	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031151FRT5
213	3	R2B5,R2B7,R2B8	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD1502F
214	1	R2B6	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD122J
215	2	R2F5,R9G3	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD222J
216	9	R2G1,R2G2,R3G1-R3G3,R4G3-R4G5,R5G1	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD560J
217	9	R2H8,R3C2,R5D4,R6E4,R6F3,R6F4,R7A30,R7E10,R7G12	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031000FRT5
218	4	R2H9,R3H10,R6B5,R9J1	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD101J
219	14	R2J1,R3C1,R3H1,R3H2,R5D2,R6B11,R6B14,R6B16,R6B19,R6B21,R6B24,R6F5,R6F9,R7B2	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW060349R9FRT5
220	21	R2J4,R2J5,R4G1,R4G2,R4G6,R4G7,R6B6,R6B8,R6B10,R6B26,R6B28,R6C1,R6C6,R6H2,R6H3,R7B4,R9D3-R9D6,R9H10	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD330J
221	1	R3D2	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD301J
222	4	R3J4,R8F2,R8G10,R9H6	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD223J
223	2	R4E1,R5D7	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD24R9F
224	4	R4E2,R4E3,R6F2,R6F10	RESN_603	PANASONIC INDUSTRIAL	ERJ3EKF60R4A
225	2	R4J3,R4J5	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031501FRT5
226	4	R4J4,R6E9,R6E10,R6G1	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031001FRT5
227	1	R5D1	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06033010FRT5
228	1	R5D6	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031370FRT5
229	2	R5F1,R6D2	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD1R0J

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 13 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
230	6	R6B12,R6B13,R6B17,R6B18,R6B20,R6B23	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD27R4F
231	1	R6B25	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD4750F
232	8	R6C12,R6C16,R7G5,R7G7,R8G1,R9D7,R9G12,R9G13	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD822J
233	5	R6C19,R6C20,R6E11,R8H9,R8H10	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD470J
234	10	R6C21,R6D1,R6D3,R6D4,R6E7,R6E8,R7E1-R7E4	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD682J
235	1	R6D5	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD40R2F
236	1	R6E1	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031300FRT5
237	2	R6E6,R7F13	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD68R1F
238	1	R7A29	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06031240FRT5
239	1	R7A31	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD5620F
240	1	R7A32	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD6190F
241	1	R7E7	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD104J
242	1	R7E8	RESN_603	KOA SPEER ELECTRONICS	RK73H1JTDD22R6F
243	3	R7F10,R7G1,R7G2	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD620J
244	3	R7F11,R8G7,R8G9	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD106J
245	1	R7F9	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW06032260FRT5
246	1	R7G13	RESN_603	VISHAY- DALE ELECTRONICS INC	CRCW060310R0FRT5
247	1	R8G12	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD334J
248	1	R8H2	RESN_603	KOA SPEER ELECTRONICS	RM73B1JTDD332J
249	9	R1B4,R3B2,R3B4,R4B2,R4B4,R4H1,R4J2,R5B4,R5C3	RESN_805	VISHAY- DALE ELECTRONICS INC	CRCW08052R2JRT5
250	10	R1B7,R3B3,R3H12,R4B3,R4H3,R5C1,R7H9-R7H12	RESN_805	ROHM CORPORATION	MCR10EZHMJ000
251	1	JA5A1	RJ45_MJ2_TH	FOXCONN ELECTRONICS, INC.	UB11123-L21

Table 14. Bill of Materials for Third Party Manufactured Parts (Sheet 14 of 14)

LI	Qty	Reference	Description	Manufacturer	Manufacturer P/N
252	87	RP1,RP1A1,RP1A2,RP1D1,RP1D2,RP1G1,RP1H1,RP1H2,RP1J1,RP2F1-RP2F5,RP2G1-RP2G5,RP2J1,RP2J2,RP3A1,RP3A2,RP3F1-RP3F3,RP3G1-RP3G5,RP4A1-RP4A3,RP4F1,RP4F2,RP4G1-RP4G5,RP4J1,RP4J2,RP5F1-RP5F4,RP5G1-RP5G7,RP6F1,RP6F2,RP6G1,RP6G2,RP7B1-RP7B5,RP7C1-RP7C3,RP7D1,RP7F1,RP8A1,RP8B2,RP8C1-RP8C4,RP8D1,RP8E1,RP8E2,RP9A1-RP9A3,RP9D1,RP9D2,RP9H1,RP9H2,RP9J1-RP9J3	RPAK4C-4R_SM		
253	4	U1B1,U5H1,U7H1,U8B2	SI4501DY_SOIC	SILICONIX	SI4501DY
254	1	U1	SPKR_TH	CHALLENGE ELECTRONICS*	DBX-05A
255	8	MH1B1,MH1G1,MH1J1,MH7A1,MH7G1,MH7J1,MH8A1,MH9G1	STD_MTG_HOLE_TH		
256	2	J8J2,J9J2	SWSPSTPB_SM_SM	E-SWITCH*	TL3304AF160QJ
257	2	DB3G1,DB3G2	TDR_PIN_TP		
258	1	RT2B1	THERMISTOR_0603	VISHAY- DALE ELECTRONICS INC	NTHS0603N02N6801JR
259	4	RT1A1,RT2A1,RT5B1,RT7H1	THERMISTOR_1812	RAYCHEM CORPORATION	MINISMDC150-2
260	1	RT4A1	THERMISTOR_1812	RAYCHEM CORPORATION	MINISMDC110-2
261	1	U9E1	TPPM0111_SOIC	TEXAS INSTRUMENTS	TPPM0111
262	1	U4J1	TPPM0115_SOIC	TEXAS INSTRUMENTS	TPPM0115DR
263	84	TS01-TS78,TS80,TS81,TS83,TS84,TS86,TS87	TRACK_SPLITTER		
264	1	CR1A1	TVS6_2V_SM	PHILIPS COMPONENTS	BZA462A125
265	1	CR4B1	TVS6_2V_SM	PHILIPS COMPONENTS	BZA462A
266	1	U7J1	VREGEZ1086_TO263	SEMTECH CORPORTION	EZ1086CM-3.3 TR
267	1	Y8G1	XTAL_HLDR_TH	PROFESSIONAL TOOLS & DIES*	A52705-003
268	1	CR1C1	ZENER_SOT23	SEMICONDUCTOR COMPONENTS INDUSTRIES LLC	MMBZ5235BLT1

Schematics B

Schematics are provided for the following items listed below. Schematics are available from the Intel Developer's Web site in PDF format.

- Block diagram
- 478 pin socket
- VTT decoupling
- Clock generator
- GMCH Part 1 and 2
- DIMM 1 and 2
- AGP
- VGA connector
- ICH4
- PCI 1, 2, and 3
- FWH & UDMA100 IDE
- USB
- AC97 CODEC
- Audio I/O
- Super I/O and FDC
- Serial, parallel, WOL and WOR
- PS/2, game and IR
- Front Panel & CNR
- ATX Power & H/W Monitor
- Voltage Regulators
- System Configuration
- PU/PDR and unused gates
- Decoupling capacitors
- Internal debug headers
- Thermtrip

This page intentionally left blank.

[FULL_ID=1164-1-16390] [PAGE_INFO_ID=16390] [MODULE_ID=1164-1-16390] [DONOR_ID=1164-1-16390]

PAGE #	COMPONENT/FUNCTION
1	COVER PAGE.
2	TABLES: BLOCK DIAGRAM
3	TABLES: RESET MAP
4	TABLES: CLOCK DISTRIBUTION
5	TABLES: GPIO/IDSEL MAPPING
6	TABLES: VOLTAGE DISTRIBUTION
7	CORE: CK_408 (MAIN CLOCK GENERATOR)
8	CORE: CPU CONNECTOR
9	CORE: CPU PULLUPS & PULLDOWNS /VCCPVID, VCC_VIDGD
10	CORE: CPU ANALOG FILTER
11-13	CORE: 82845GV GMCH
14	INTENTIONALLY LEFT BLANK
15	CORE: 82845GV DECOUPLING & REFERENCE VOLTAGES
16	CORE: DDR SERIES TERMINATION
17	CORE: DIMM CONNECTORS
18-19	CORE: DDR PARALLEL TERM (STROBES, CNTL)
20	CORE: DDR VTERM CAPS
21	CORE: DEBUG CONNECTOR
22	CORE: VGA CONNECTOR (DFM29)
23-24	ICH: 82801DB I/O CONTROLLER HUB
25	ICH: ICH PULL-UP/PULL-DOWNS
26	ICH: LAN LINK
27	ICH: IDE PRIMARY & SECONDARY
28	ICH: USB BACK PANEL CONNECTORS
29	ICH: USB CNR/SIO STUFFING OPTION (DFM29)
30	ICH: USB FRONT PANEL/CNR VREG & OC#,
31-33	ICH: PCI SLOTS 3 - 1
34	ICH: PCI PULL-UPS
35	SMBUS ISOLATION
36	CNR CONNECTOR
37	LAN: KINNERETH+
38	AUDIO: CODEC (AD1885 OR CS4201)
39	AUDIO: CODEC FILTERING CAPS
40	AUDIO: AUX-IN, CD-IN, LINE-IN: ATAPI HEADERS
41	AUDIO: MIC-IN
42	AUDIO: LINE-OUT
43	AUDIO: FRONT PANEL AUDIO HEADER
44	AUDIO: TRANSIENT CONTROL
45	AUDIO: ANALOG VREG
46	SIO: LPC47M102
47	SIO: FLOPPY
48	SIO: KEYBOARD & MOUSE PORTS (PS/2) (DFM29)
49	SIO: PARALLEL PORT (DFM29)
50	SIO: COM1 (DFM29)
51	FWH: MFG MODE AND RECOVERY JUMPERS
52	GLUE4
53	HECETA4 & HECETA6
54	PC SPEAKER
55	FRONT PANEL HEADER
56	LABELS / MOUNTING HOLES
57	FAN: FAN HEADERS (3)
58	VREG: 2.5V MEMORY, STANDBY-MEMORY
59	VREG: 1.25V MEMORY VTT
60	VREG: POWER CONNECTOR 2X10
61	VREG: BATTERY, PCI VAUX, USB_NCH & USB_PCH
62	VREG: USB BACK PANEL, PS/2
63	VREG: 1.5V STBY & 3.3V STBY
64	VREG: BULK DECOUPLING
65	VREG: 2.5V STR DECOUPLING
66	VREG: CORE 1.5V
67	VREG: CPU MAIN REGULATOR (VCCP)
68	VREG: CPU DECOUPLING, 12V CONN/FILTER INDUCTOR
69	DCL TRACK SPLITTERS
70	DEBUG: TITLE PAGE
71	DEBUG: ITP PORT AND PULL-UPS
72	MOON ISA RESISTORS
73	INTENTIONALLY LEFT BLANK
74	DEBUG: DIAGNOSTIC LEDS , JUMPERS (H_VID)
75	DEBUG: PORT80 DECODER
76	DEBUG: TDR COUPONS, , HUBLINK LAI, POC HDR, RESISTIVE LOADS
77	DEBUG: DIAGNOSTIC JUMPERS (SMI, STPCLK)

#1 = SCHEMATIC SUPPORTS GMCH REV1.5 FOOTPRINT
PAGE 14 ONLY FOR BALLOUT 1.0 COMPATIBILITY

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
1.0	PRELIMINARY		9/01				

PBA C23015-001

INTEL® 845GV SCALABLE PERFORMANCE BOARD

COPIED FROM: REV 0.85 OF NBVV_DDR 2/15/01

FAB D

REV 4.0

TAPE-OUT:
2-08-02

POWER SYMBOLS USED:
VCC3
VCC
+12V
-12V

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL'S FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
5. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

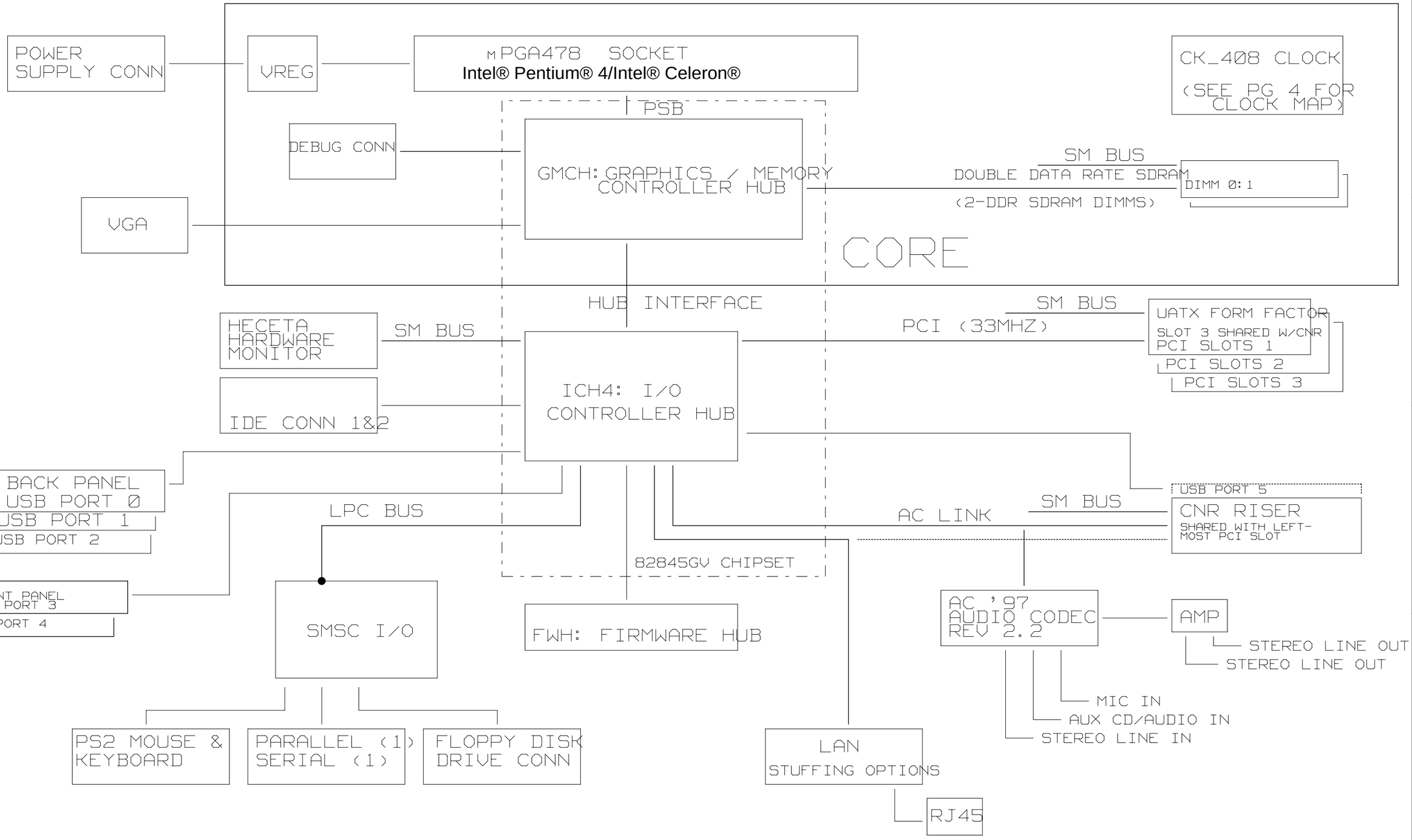
DRAWING
BROOKDALE_G.SCH.1.1
Mon Nov 25 14:13:59 2002

WMT SKT-N/82845GV VALIDATION VEHICLE
2-DDR SDRAM; 4 LAYER; uATX

BOM RELEASE DATE		PB NUMBER C23015-001		
SIGNATURE	DATE	intel	3065 BOWERS AVE SANTA CLARA, CA 95051	
DRN BY				
CHK BY BGRVP TEAM		TITLE SCH, PBA, BGRVP_DDR		
ENGR APVD				
APVD			DOCUMENT NUMBER C23021	PAGE 1 / REV 4.0
APVD				

[DONOR_REV=0.07/page8] [DONOR_PROJ=wtvv_pdt] [PROJ_REV=2.00/page1] [PROJ_NAME= :_G_DDR--1164] [MODULE=CORES] [MOD_REV=0.05] [MOD_PAGE=page1] [PAGE_TITLE=INDEX] [LAST_MAKEPROJ: 10/12/2001 1:56:32 PM] [LAST_MAKEGOLD: 10/17/99 6:44:38pm] [SOLUTION=PERFORMANCE/WTVV]

[FULL_ID=1164-2-[illegible] [MODULE_ID=128-2-[illegible]



BLOCK DIAGRAM VALID PER 09/21 DESIGN

DRAWING
BGRVP.SCH_1.2
Tue Nov 19 14:27:00 2002

	DOCUMENT NUMBER	PAGE	REV
	C23021	2	4.0

[DONOR_REV=1.02/page2] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page2] [PROJ_NAME=[illegible]_G_DDR--1164] [MODULE=CORES] [PAGE_TITLE=CLOCK] [SOLUTION=PERFORMANCE/WTVV] [MOD_PAGE=page2] [LAST_MAKEPROJ: 10/12/2001 1:56:32 PM] [LAST_MAKEGOLD: 10/17/99 6:44:41pm] [MOD_REV=0.05]

CORE

AFTER P_PCIRST*, HANDSHAKE (ON HI BUS) BETWEEN GMCH/ICH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED

GMCH: GRAPHICS/MEMORY CONTROLLER HUB
RSTIN*
PWROK
H_CPURST*

V-LEVEL — DBG_CPURST — LED, POC PLD

RESET*
H_PWRGD
MPGA478 SOCKET

P_PCIRST*

FWH_RST*
FWH; FIRMWARE HUB

SIO_PCI_RST*
SMC I/O KBRST*

SLOTS_P_RST*
PCI SLOT 1
PCI SLOT 2
PCI SLOT 3

SLOTS_P_RST*
AGP4X
AGP CONN
CORE

POWER SUPPLY CONN
PS_ON* PWRGD_PS

H_PWRGD
P_RST_SLOTS*
AUD_RST*
P_PCIRST*
PWRGD_PS
PWRGD_3V
RSMRST*
PS_ON*
GLUECHIP4
FP_RST*
IDE_RST*
SLP_S5*
SLP_S3*

RSMRST*

IDE_RST*
IDE CONN1
IDE CONN2

CPU: DBRESET (ITP)
DBR*
CORE

FRONT PANEL CONN
FP_RST*
SW_ON*

FWH
WAKE USB

PWRGD_3V
RSMRST*
H_PWRGD
SYS_RST*
SW_ON*
KBRST*
P_PCIRST*
AUD_LINK_RST*
ICH_LAN_RST
ICH4: I/O CONTROLLER HUB
SLP_S5*
SLP_S4*
SLP_S3*

VREG: USB
FRNT: LED

BUFFER — P_PCIRST_DEBUG* — PORT 80, POC PLD, LAI HDR
BUFFER — DEBUG LED

AC97 AUDIO CODEC
AUD_LINK_RST*
RES (OPTION)
DYNAMIC PRIMARY DOWN CNTL

CNR (SHARED SLOT)
AUD_LINK_RST*
ICH_LAN_RST

LAN
ICH_LAN_RST

RESET MAP

DRAWING
BGRVP.SCH_1.3
Mon Nov 18 13:06:37 2002

DOCUMENT NUMBER	PAGE	REV
C23021	3	4.0

[FULL_ID=1164-4-1BGRVP] [INFO_ID=16396] [MODULE_ID=128-4-1BGRVP] [DONOR_ID=1130-4-15452]

3.3 VOLT

14.318MHZ

SUSCLK 32.7KHZ

LANCLK 5 - 50 MHZ

(INPUT FROM LAN/CNR)

EECLK

32.7KHZ

ICH

AUD_BCLK

LAN

AUDIO CODEC

24.5MHZ

AUD_BCLK

12.288 MHZ

SIO

CNR CON

AUDIO

FWH

33MHZ PCI SLOT 3

33MHZ PCI SLOT 2

33MHZ PCI SLOT 1

33MHZ

33MHZ

33MHZ

33MHZ

3.3 VOLT

48MHZ

GLUECHIP

POC PLD

CK408

HUB INTERFACE LAI

66MHZ

66MHZ

66MHZ

66MHZ

66MHZ

48MHZ

66MHZ INPUT TEST POINT

DEBUG CON

6 DDR CLK PAIRS 100/133 MHZ

GMCH

DIMM0

DIMM1

0

1

2

3

4

5

14.318MHZ

VREG

VTT_PWRGD

HOST CLOCK PAIRS 100/133 MHZ

GMCH_CK

CPU_CK

ITP_INTERPOSER_CK

CPU

CORE

ITP CORE

ITP PORT

CORE

INFORMATION UPDATED (DESIGN AS OF 9/14)

CLOCK DISTRIBUTION

DRAWING BGRVP.SCH_1.4 Tue Nov 19 14:27:27 2002

DOCUMENT NUMBER	PAGE	REV
C23021	4	4.0

[DONOR_REV=1.02/page4] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page4] [PROJ_NAME=G_DDR--1164] [MOD_REV=0.05] [MODULE=CORE] [PAGE_TITLE=CLOCK_DISTRIBUTION] [MOD_PAGE=page6] [SOLUTION=PERFORMANCE/WTVV] [LAST_MAKEPROJ: 10/12/2001 1:55:32 PM] [LAST_MAKEGOLD: 10/17/99 6:45:16pm]

ICH4

PIN NAME	PWR WELL	USAGE	DURING RESET	S3/S4/S5	INTERNAL PULL-UP	NOTES
GPI(0)	CORE	P_REQA#	---	---		
GPI(1)	CORE	P_REQ5#	---	---		
GPI(2)	CORE	P_IRQE#	---	---		
GPI(3)	CORE	P_IRQF#	---	---		
GPI(4)	CORE	P_IRQG#	---	---		
GPI(5)	CORE	P_IRQH#	---	---		
GPI(6)	CORE	UNUSED	---	---		
GPI(7)	CORE	UNUSED	---	---		
GPI(8)	RESUME	UNUSED	---	---		
GPI(11)	RESUME	SMB_ALERT#	---	---		
GPI(12)	RESUME	LPC_SIO_SMI#	---	---		
GPI(13)	RESUME	LPC_SIO_PME#	---	---		
GPO(16)	CORE	P_GNTA#	HIGH	OFF	24K	
GPO(17)	CORE	P_GNT5#	HIGH	OFF	24K	
GPO(18)	CORE	UNUSED	HIGH	OFF		
GPO(19)	CORE	UNUSED	HIGH	OFF		
GPO(20)	CORE	UNUSED	HIGH	OFF		
GPO(21)	CORE	ISA_GO_NOGO	HIGH	OFF		
GPO(22)	CORE	UNUSED	HIGH-Z	OFF		
GPO(23)	CORE	UNUSED	LOW	OFF		
GPIO(24)	RESUME	UNUSED	LOW	DEFINED		
GPIO(25)	RESUME	GPO_GRN_BLNK	HIGH	DEFINED		
GPIO(27)	RESUME	GPO_YEL_BLNK	HIGH	DEFINED		
GPIO(28)	RESUME	GPO_LAN_DISABLE	HIGH	DEFINED		
GPIO(32)	CORE	NO_POP*	HIGH	OFF		
GPIO(33)	CORE	UNUSED	HIGH	OFF		
GPIO(34)	CORE	UNUSED	HIGH	OFF		
GPIO(35)	CORE	UNUSED	HIGH	OFF		
GPIO(36)	CORE	UNUSED	HIGH	OFF		
GPIO(37)	CORE	(BOARD1)	HIGH	OFF		
GPIO(38)	CORE	(BOARD2)	HIGH	OFF		
GPIO(39)	CORE	(BOARD3)	HIGH	OFF		
GPIO(40)	CORE	(BOARD4)	HIGH	OFF		
GPIO(41)	CORE	UNUSED	HIGH	OFF		
GPIO(42)	CORE	UNUSED	HIGH	OFF		
GPIO(43)	CORE	CDC_DWN_ENAB*	HIGH	OFF		
RI*	RESUME					
THERM*	CORE					

FWH

GPI4		CONFIG JUMPER	INPUT	DEFINED		CONFIG JUMPER
GPI3		MANUF MODE	INPUT	DEFINED		MANUF MODE
GPI2		HI/LOW BIOS CONFIG	INPUT	DEFINED		SPARE HI/LOW BIOS CONFIG STRAP
GPI1		GPIO_DMA66_DETECT_SEC	INPUT	DEFINED		ATA66 CABLE DETECT - SECONDARY
GPI0		GPIO_DMA66_DETECT_PRI	INPUT	DEFINED		ATA66 CABLE DETECT - PRIMARY

SIO

GPIO20		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING
GPIO21		RESISTOR STRAP OPTION	INPUT	DEFINED		DESIGN FEATURE WITH RESISTOR STRAPPING
GP027/IOSMI*		IO_SMI*	INPUT	DEFINED		SENDS IO SMI REQUEST TO ICH2

MULTI-PLEXED GPIO PINS ON SIO USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
UN-USED GPIO PINS ON SIO ARE NOT IDENTIFIED HERE

IRQ ROUTING TABLE

	AGP	SLOT1	SLOT2	SLOT3	AC97/ SMBUS	USB 2.0	USB 1.1 #1	USB 1.1 #2	USB 1.1 #3	LAN
INT A	A			D			A			
INT B	B			C	A					
INT C				A					A	
INT D				B				A		
INT E		D	C							A
INT F		A	B							
INT G		B	A							
INT H		C	D			A				
REG /GNT										
IDSEL		16	17	18						24

GPIO, IRQ, IDSEL MAPS

DRAWING
BGRVP.SCH_1.5
Mon Nov 18 13:47:40 2002

DOCUMENT NUMBER	PAGE	REV
C23021	5	4.0

[PAGE_TITLE=BLOCK_DIAGRAM]

ATX P/S WITH 1A 5VSB

ATX 12V P/S

5VSB
5V
3.3V
+12V
-12V

+12V

VRM 9.0
PG 67,68

VCC_VID VREG
PG 9

GMCH VTT
PSB I/O:
1.15-1.75V
2.4 A
S0, S1

MPGA478
VCCP
60 A, S0, S1
VCC_VID
30 MA, S0, S1

ICH4
VCCCPU-VRM OUT
?MA
S0, S1

VCCCORE:
CORE LOGIC:
1.5V
1.06 A
S0, S1

VCCHI:
HI I/O:
1.5V
90 MA
S0, S1

VCC3_3:
3.3V
610 MA
S0, S1

VCC3

V_5P0_STBY
1.5VSB REGULATOR
PG 63
V_1P5_STBY

VCCSUS1_5-ICH
RESUME:
1.5V
85 MA S0, S1
85 MA S3, S5

V_5P0_STBY
3.3VSB REGULATOR
PG 63
V_3P3_STBY

VCCSUS3_3-ICH
RESUME:
3.3V
70 MA S0, S1
70 MA S3, S5

OR

VCCRTC-ICH RTC:
VBAT
5UA
S0, S1, S3, S5

BATTERY
PG 61

V_3P3_STBY

1.5V REGULATOR
PG 66
V_1P5_CORE

V_2P5_CORE

VCC
2.5V REGULATOR
PG 58

VSB REGULATOR

PG 58
V_2P5_SM

1.25V REGULATOR
PG 59
V_1P25_MEMVTT

VCC
PG 30
V_USB_PWR_CNR

V_3P3_PCIAUX
VCC3
V_3P3_STBY
PG 61

GMCH

VCCHI, HI I/O:
1.5V
90 MA, S0, S1

VCC, CORE LOG.
1.5V
2.46 A, S0, S1

VCCAGP, AGP I/O
1.5V
370 MA, S0, S1

VCCDAC, DAC I/O
1.5V
65 MA, S0, S1

VCCGPIO
3.3V
30 MA, S0, S1

VCCSM, DDR I/O
2.5V
2.8 A S0, S1
95 MA S3

DDR 2 DIMMS:
2.5V
5.02 A S0, S1
138 MA S3

DDR VTT
1.25V
2.1 A S0, S1
0 MA S3

PCI PER SLOT:
3.3V 7.6 A
5V 5 A
+12V 0.5 A
-12V 0.1 A

PCI 3.3VAUX PER SLOT:
3.3V
1A S0, S1
475MA S3, S5

CNR CONNECTOR POWER:
3.3V 1 A
3.3V 1 A DUAL
5V 1 A
5V 0.5A DUAL
+12V 0.5 A
-12V 0.1 A

VCC3

CK_408:
3.3V
280 MA S0, S1

V_3P3_STBY
VCC3

LPC SUPER I/O:
3.3V
25 MA S0, S1

FWH CORE:
3.3V
67MA S0, S1

VREG_USB_BPL
VREG_USB_BPR
VREG_PS2

VCC
V_5P0_STBY
PG 62

USB AND PS/2 CABLE POWER:
5V
500MA * 6 S0, S1
1MA S3, S5

+12V
AUDIO SPO
PG 45

AC'97 AUDIO CODEC:
5V
?A S0, S1
0A S3, S5

VCC3

V_1P5_CORE
VCC3
VCC
+12V

DEBUG CONNECTOR
1.5V 2.0A
3.3V 6A
5V 2A
+12V 1A

-12V
+12V
VCC3
VCC
V_5P0_STBY

_DRAWING
BGRVP.SCH_1.6
Tue Nov 19 14:45:54 2002

DOCUMENT NUMBER	PAGE	REV
C23021	6	4.0

ROOM=DCL_CORE_CLK

NOTE:
BSEL[1:0] OF THE CPU
DO NOT CORRESPOND DIRECTLY
TO THE CK-408 SEL[1:0]

SEL_2	SEL_1	SEL_0	FUNCTION
0	0	0	66 MHZ HOST CLOCK
0	0	1	100 MHZ HOST CLOCK
0	1	0	200 MHZ HOST CLOCK
0	1	1	133 MHZ HOST CLOCK
1	X	X	SEE CK-408 CLOCK SPEC
MID	0	0	ALL OUTPUTS HI-Z
MID	0	1	TEST MODE
MID	1	0	SEE CK-408 CLOCK SPEC
MID	1	1	SEE CK-408 CLOCK SPEC
			MID = 1.0V TO 1.8V

SMB ADDRESS
1101001O
D2 WRITE
D3 READ

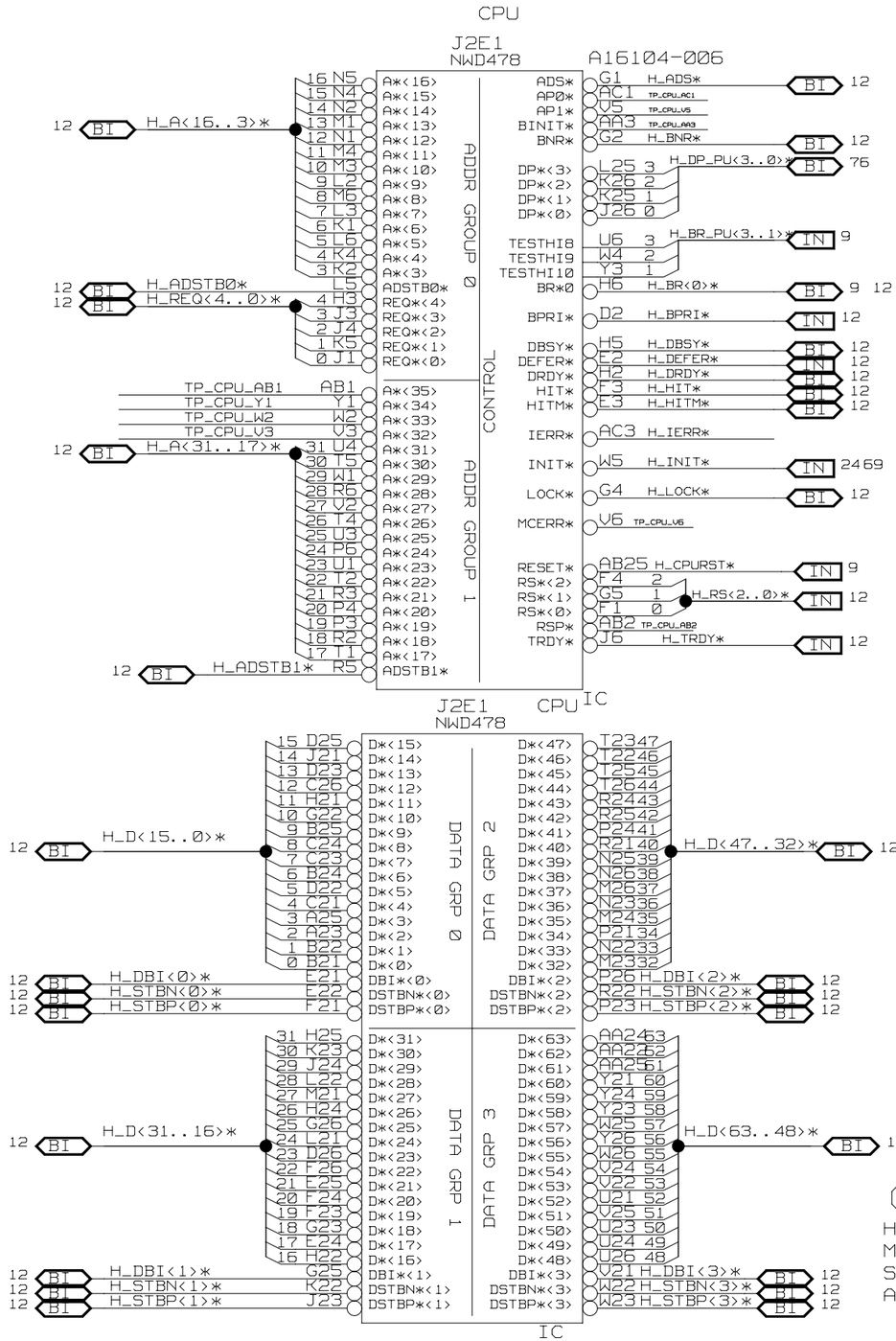
CAD NOTE:
TIE VSSA (U3F1-27)
DIRECTLY TO C13G4

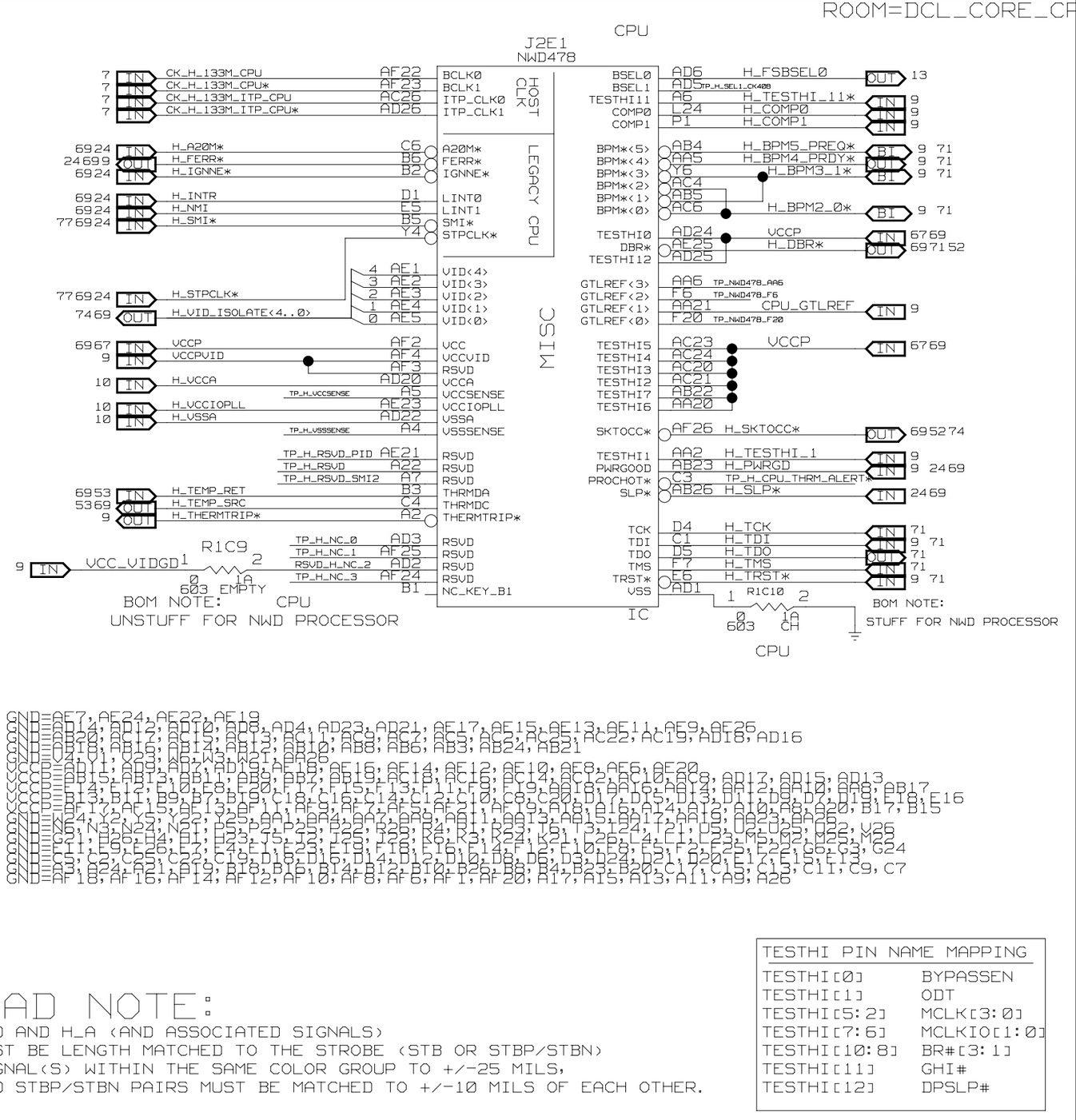
SPARE SECTIONS

DRAWING
BGRVP.SCH_1.7
Mon Nov 18 13:48:18 2002

DOCUMENT NUMBER	PAGE	REV
C23021	7	4.0

ROOM=DCL_CORE_CPU





GND=AE7,AE24,AE22,AE19
GND=AD14,AD12,AD10,AD8,AD4,AD23,AD21,AE17,AE15,AE13,AE11,AE9,AE26
GND=AB20,AC17,AC15,AC13,AC11,AC9,AC7,AC5,AC2,AC25,AC22,AC19,AD18,AD16
GND=AB18,AB16,AB14,AB12,AB10,AB8,AB6,AB3,AB24,AB21
GND=AA4,Y1,X23,W6,W3,W21,AA26
GND=AB1,AB7,AB9,AB11,AB13,AB15,AB17,AB19,AE16,AE14,AE12,AE10,AE8,AE6,AE20
GND=AB15,AB13,AB11,AB9,AB7,AB5,AB3,AB1,AC18,AC16,AC14,AC12,AC10,AC8,AD17,AD15,AD13
GND=F14,F11,F10,F8,F7,F20,F17,F15,F13,F12,F10,F9,F7,AB18,AA16,AA14,AA12,AA10,AA8,AB17
GND=F18,F16,F12,F9,F6,F3,F19,F5,F4,AA18,AA16,AA14,AA12,AA10,AA8,AA6,AB19,AB16,AB15
GND=AF1,Y2,AF15,Y20,F13,Y3,AF11,AF9,AF7,AF5,AF3,AF19,AF17,AA19,AA17,AA15,AA13,AA11,AA9,AA7,AA5,AA3,AB2,AB4,AB20,AB22,AB24,AB26
GND=L4,Y5,Y22,AA1,AA24,AA26,AB25,AB23,AB21,AB17,AB15,AB13,AB11,AB9,AB7,AB5,AB3,AB1
GND=G6,N3,N24,N21,P5,P2,P25,P22,R20,R4,R1,R23,T6,T3,T24,T21,U5,U2,U25,U22,V26
GND=F21,E26,H4,H1,H23,J5,J2,J25,J22,K6,K3,K24,K21,L26,L4,L1,L23,M5,M2,M25,M22
GND=H11,F9,L26,L7,F4,E1,E23,F18,F16,F14,F12,F10,F8,F5,F2,F22,F25,E22,C6,C3,G24
GND=C5,C2,C25,C22,C19,D18,D16,D14,D12,D10,D8,D6,D3,D24,D21,D20,E17,E15,E13
GND=B3,B24,A21,B19,B16,B15,B14,B12,B10,B20,B8,B4,B23,B20,C17,C15,C13,C11,C9,C7
GND=AF18,AF16,AF14,AF12,AF10,AF8,AF6,AF1,AF20,A17,A15,A13,A11,A9,A26

TESTHI PIN NAME MAPPING	
TESTHI[0]	BYPASSEN
TESTHI[1]	ODT
TESTHI[5:2]	MCLK[3:0]
TESTHI[7:6]	MCLKIO[1:0]
TESTHI[10:8]	BR#[3:1]
TESTHI[11]	GHI#
TESTHI[12]	DPSLP#

CAD NOTE:

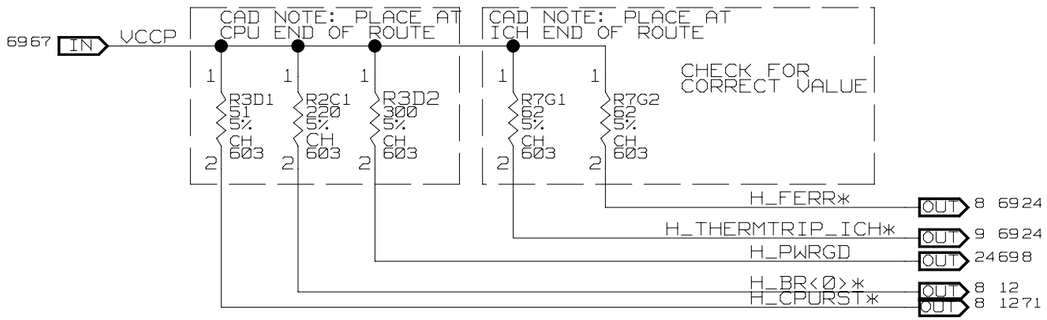
H_D AND H_A (AND ASSOCIATED SIGNALS)
MUST BE LENGTH MATCHED TO THE STROBE (STB OR STBP/STBN)
SIGNAL(S) WITHIN THE SAME COLOR GROUP TO +/-25 MILS,
AND STBP/STBN PAIRS MUST BE MATCHED TO +/-10 MILS OF EACH OTHER.

CPU CONNECTOR (SOCKET 478)

DRAWING
BGRVP.SCH 1.8
Mon Nov 25 12:48:06 2002

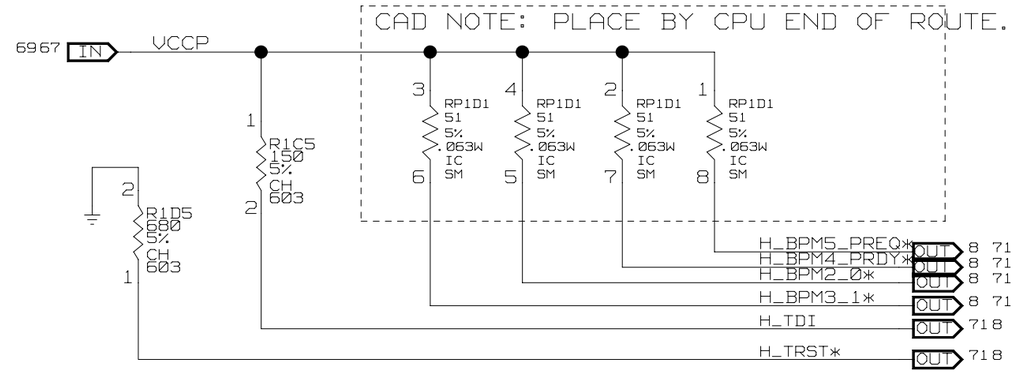
DOCUMENT NUMBER	PAGE	REV
C23021	8	4.0

CPU SIGNAL TERMINATION



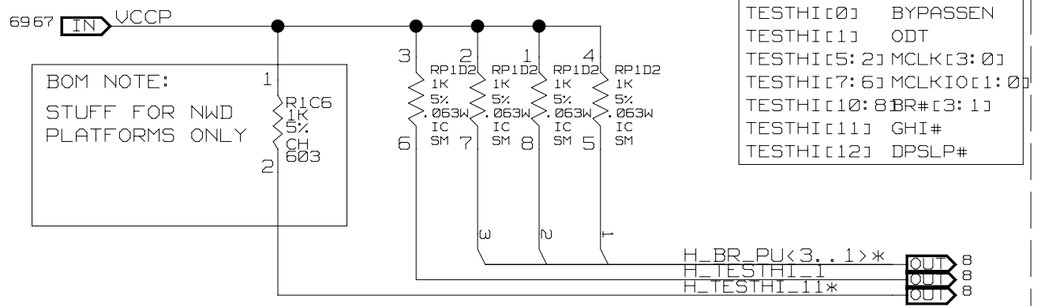
ROOM=DCL_CORE_CPU

ITP/TAP TERMINATION



CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET

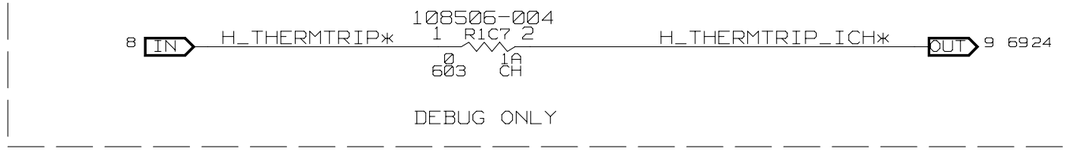
TESTHI PULLUPS



TESTHI PIN NAME MAPPING

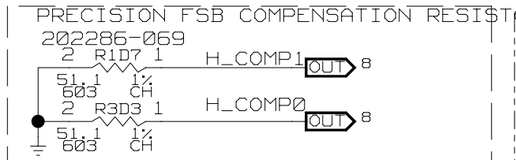
TESTHI[0]	BYPASSEN
TESTHI[1]	ODT
TESTHI[5:2]	MCLK[3:0]
TESTHI[7:6]	MCLKIO[1:0]
TESTHI[10:8]	BR#[3:1]
TESTHI[11]	GHI#
TESTHI[12]	DPSLP#

DESIGN NOTE: THESE CAN BE COST-REDUCED FOR PRODUCTION
BY GROUPING [11], [10:8], AND [1:0] TO ONE PULLUP PER GROUP



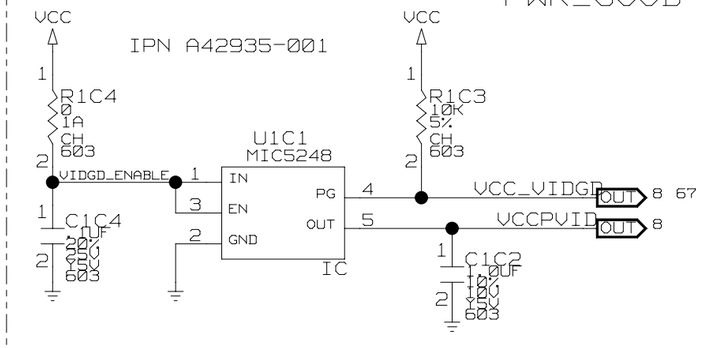
DEBUG ONLY

PRECISION FSB COMPENSATION RESISTORS



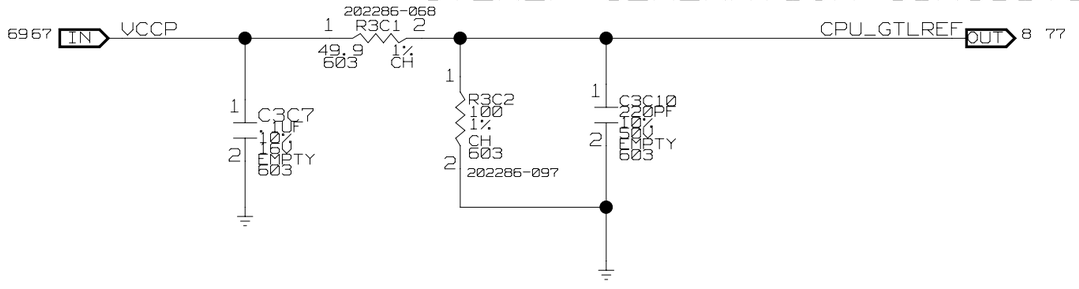
PLACE THESE OUTSIDE SOCKET CAVITY

PWR_GOOD



PLACE NEAR PIN 5

GTLREF GENERATION CIRCUITS



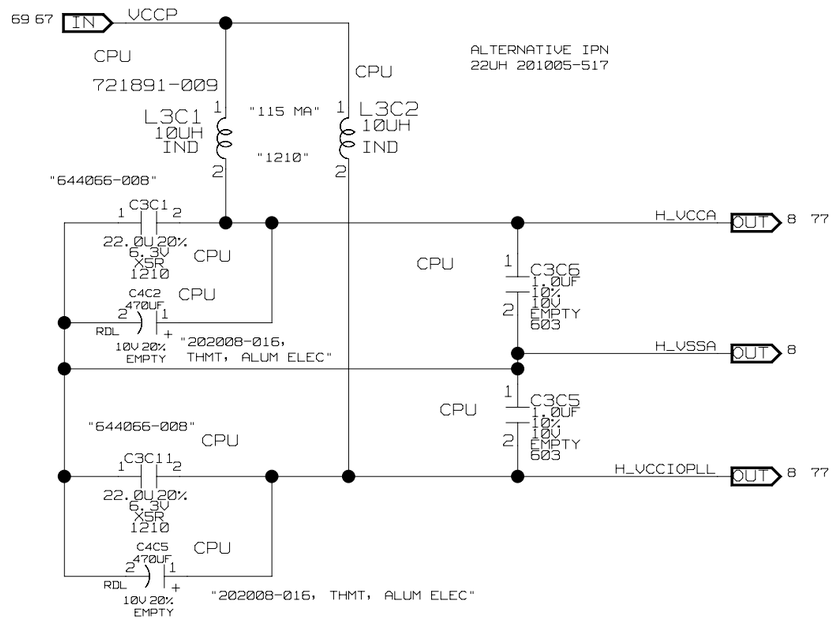
CPU PULLUPS/PULLDNS/TERMINATION

DRAWING
BGRVP.SCH_1.9
Mon Nov 18 13:48:08 2002

DOCUMENT NUMBER	PAGE	REV
C23021	9	4.0

ROOM=DCL_CORE_GMCH

PLL SUPPLY FILTER



CAD NOTE:

PLACE THMT CAPS OUTSIDE RM BOUNDARY.
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

CAD NOTE: PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

FILTERED ANALOG SUPPLY

DRAWING
FAB_A.SCH.1.10
Mon Nov 18 13:48:27 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	10	4.0

ROOM=DCL_CORE_GMCH

NOTE:
HEATSINK ASSM WITH GASKET # A67625-001
HEATSINK ASSM WITH NO GASKET # A67916-001

U6D1 DCL_CORE_GMCH
BDG_DDR_2P0

SMAA0 REV 2.0
SMAA1
SMAA2
SMAA3
SMAA4
SMAA5
SMAA6
SMAA7
SMAA8
SMAA9
SMAA10
SMAA11
SMAA12

SMAB1
SMAB2
SMAB4
SMAB5

SWE*
SCAS*
SRAS*

SBA0
SBA1

SCS0*
SCS1*
SCS2*
SCS3*

SCKE0
SCKE1
SCKE2
SCKE3

SCMD_CLK0
SCMD_CLK0*
SCMD_CLK1
SCMD_CLK1*
SCMD_CLK2
SCMD_CLK2*
SCMD_CLK3
SCMD_CLK3*
SCMD_CLK4
SCMD_CLK4*
SCMD_CLK5
SCMD_CLK5*

SRCVEN_OUT*
SRCVEN_IN*

SDQS0 SDM0 SDQ0 SDQ1 SDQ2 SDQ3 SDQ4 SDQ5 SDQ6 SDQ7
SDQS1 SDM1 SDQ8 SDQ9 SDQ10 SDQ11 SDQ12 SDQ13 SDQ14 SDQ15
SDQS2 SDM2 SDQ16 SDQ17 SDQ18 SDQ19 SDQ20 SDQ21 SDQ22 SDQ23
SDQS3 SDM3 SDQ24 SDQ25 SDQ26 SDQ27 SDQ28 SDQ29 SDQ30 SDQ31
SDQS4 SDM4 SDQ32 SDQ33 SDQ34 SDQ35 SDQ36 SDQ37 SDQ38 SDQ39
SDQS5 SDM5 SDQ40 SDQ41 SDQ42 SDQ43 SDQ44 SDQ45 SDQ46 SDQ47
SDQS6 SDM6 SDQ48 SDQ49 SDQ50 SDQ51 SDQ52 SDQ53 SDQ54 SDQ55
SDQS7 SDM7 SDQ56 SDQ57 SDQ58 SDQ59 SDQ60 SDQ61 SDQ62 SDQ63

1 OF 5
IC

M_DQ<63..0> BI 16
M_DQS<7..0> BI 16
M_DM<7..0> BI 16

M_MAA_CPC<5..1> OUT 19 17
M_MAA<12..0> OUT 18 17
M_MAB_CPC<5..1> OUT 19 17
M_WE* OUT 19 17
M_CAS* OUT 19 17
M_RAS* OUT 19 17
M_BS<1..0> BI 19 17
M_SCS<3..0>* BI 19 17
M_SCKE<3..0> BI 19 17

CK_M_100_133M_P_DDR0 OUT 17
CK_M_100_133M_N_DDR0 OUT 17
CK_M_100_133M_P_DDR1 OUT 17
CK_M_100_133M_N_DDR1 OUT 17
CK_M_100_133M_P_DDR2 OUT 17
CK_M_100_133M_N_DDR2 OUT 17
CK_M_100_133M_P_DDR3 OUT 17
CK_M_100_133M_N_DDR3 OUT 17
CK_M_100_133M_P_DDR4 OUT 17
CK_M_100_133M_N_DDR4 OUT 17
CK_M_100_133M_P_DDR5 OUT 17
CK_M_100_133M_N_DDR5 OUT 17

TP_CS_RCLK AK24
TP_CS_OCLK AL23

NB DCL_CORE_GMCH
DIMM_VREF_1P25 IN 59 17
R6F6 2 0 603 1A CH
SMVREF_R
SM_VREF AM2
C6E13 .1UF 10% 16V X7R 603
NB

SMRCOMP1 OUT
V_2P5_SM IN 58
SMXRCOMP AF10
SMYRCOMP AJ34

CAD NOTE:
PLACE C6F3 BY
R6F2 AND R6F10

NB R4E2 60.4 1% CA 603
NB C6F3 .1UF 20% 25V Y5U 603
NB R6F2 60.4 1% CA 603

DCL_CORE_GMCH
SMRCOMP2

CAD NOTE:
PLACE C4E3 BY
R4E3 AND R4E2

NB R4E3 60.4 1% CA 603
DCL_CORE_GMCH
NB R6F10 60.4 1% CA 603

NB DCL_CORE_GMCH
U6D1
BDG_DDR_2P0
5 OF 5

G_C_BE<3..0>* BI 21
G_CBE0* R4
G_CBE1* N4
G_CBE2* M2
G_CBE3* H2

G_FRAME* BI 21 M4
CK_66M_GMCH IN 7 AE7
G_DEVSEL* BI 21 N2
G_IRDY* BI 21 N7
G_TRDY* BI 21 N5
G_STOP* BI 21 P2
G_PAR BI 21 P4
G_REQ* IN 21 D5
G_GNT* OUT 21 B5
GRCOMP B 15 L2
AGPREF_GMCH BI 21 W2

G_RBF* IN 21 G7
G_WBF* IN 21 G5
G_PIPE* IN 21 H8

G_ST<2..0> BI 21
HI<10..0> BI 76 69 24

HI_VREF_GMCH IN 69 15 AD3
HI_VSWING_GMCH IN 69 15 AD2
HI_STBS BI 76 69 24 AD4
HI_STBF BI 76 69 24 AC4
HI_RCOMP_GMCH IN 15 AC2
P_PCIRST* IN 69 25 AJ31
BG_RSVD_AB3 IN 76 AB3
BG_RSVD_AB2 IN 77 AB2

GFRAME*
GCLKIN
GDEVSEL*
GIRDY*
GTRDY*
GSTOP*
GPAR
GREQ*
GGNT*
AGPRCOMP
AGPVREF
GRBF
GWBF
GPIPE
GST0 C4
GST1 B4
GST2 B3
HI0 AA7
HI1 AB8
HI2 AC7
HI3 AC5
HI4 AD8
HI5 AF4
HI6 AE4
HI7 AE5
HI8 AF3
HI9 AE2
HI10 AF2
HI_VREF
HI_SWING
HI_STBS
HI_STBF
HI_RCOMP
RSTIN*
RSVD
RSVD

G_ADSTB0 BI 21
G_ADSTB0* BI 21
G_AD<31..0> BI 11 21
GADSTB0 V8
GADSTB0* U7
G_AD0 V4 0
G_AD1 V2 1
G_AD2 W4 2
G_AD3 W5 3
G_AD4 U5 4
G_AD5 U4 5
G_AD6 U2 6
G_AD7 V3 7
G_AD8 T2 8
G_AD9 T3 9
G_AD10 T4 10
G_AD11 R2 11
G_AD12 R5 12
G_AD13 R7 13
G_AD14 T8 14
G_AD15 P3 15

G_ADSTB1 BI 21
G_ADSTB1* BI 21
G_AD<31..0> BI 11 21
GADSTB1 M8
GADSTB1* L7
G_AD16 P8 16
G_AD17 K4 17
G_AD18 K2 18
G_AD19 J2 19
G_AD20 M3 20
G_AD21 L5 21
G_AD22 L4 22
G_AD23 H4 23
G_AD24 G2 24
G_AD25 K3 25
G_AD26 J4 26
G_AD27 J5 27
G_AD28 J7 28
G_AD29 H3 29
G_AD30 K8 30
G_AD31 G4 31

G_SBSTB BI 21
G_SBSTB* BI 21
G_SBA<7..0> BI 21
GSBSTB F4
GSBSTB* E5
GSBA0 C3 0
GSBA1 C2 1
GSBA2 D3 2
GSBA3 D2 3
GSBA4 E4 4
GSBA5 E2 5
GSBA6 F3 6
GSBA7 F2 7

IC

CAD NOTE:
SPACING FOR THE STOBES
IS 20 MILS TO DATA.

AB2	GMCH_TEST
AB3	SSI_ST

82845GV CHIPSET
PART 1 OF 3

DRAWING
FAB_A.SCH.1.11
Mon Nov 18 12:42:55 2002
DB45GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	11	4.0

ROOM=DCL_CORE_GMCH

A13494-005
RETENTION ACHOR CLIPS: QTY(4)

J6D1 HDR NB
J4F1 HDR NB
J6F1 HDR NB
J4D1 HDR NB

NB

U6D1
BDG_DDR_2P0

8 BI H_A<31..3>*
3 W31 HA3*
4 AA33 HA4*
5 AB30 HA5*
6 V34 HA6*
7 Y35 HA7*
8 AC33 HA8*
9 Y35 HA9*
10 AA36 HA10*
11 AC34 HA11*
12 AB34 HA12*
13 Y34 HA13*
14 AB36 HA14*
15 AC36 HA15*
16 AC31 HA16*
17 AF35 HA17*
18 AD36 HA18*
19 AD35 HA19*
20 AE34 HA20*
21 AD34 HA21*
22 AE36 HA22*
23 AF36 HA23*
24 AE33 HA24*
25 AF34 HA25*
26 AG34 HA26*
27 AG36 HA27*
28 AE31 HA28*
29 AH35 HA29*
30 AG33 HA30*
31 AG31 HA31*

8 BI H_REQ<4..0>*
0 V36 HREQ0*
1 AA31 HREQ1*
2 W33 HREQ2*
3 AA34 HREQ3*
4 W35 HREQ4*

8 BI H_ADSTB0* AB35 HADSTB0*
8 BI H_ADSTB1* AF30 HADSTB1*

7 IN CK_H_133M_GMCH K30 HCLKP
7 IN CK_H_133M_GMCH* J31 HCLKN
15 IN HYRCOMP V35 HYRCOMP
15 IN HYSWING Y30 HYSWNG
15 IN HXRCOMP B28 HXRCOMP
15 IN HXSWING H28 HXSWNG

8 BI H_STBP<0>* L31 HDSTBP0*
8 BI H_STBN<0>* N31 HDSTBN0*
8 BI H_DBI<0>* N33 DINV0*
8 BI H_STBP<1>* J34 HDSTBP1*
8 BI H_STBN<1>* G33 HDSTBN1*
8 BI H_DBI<1>* C35 DINV1*
8 BI H_STBP<2>* E29 HDSTBP2*
8 BI H_STBN<2>* C30 HDSTBN2*
8 BI H_DBI<2>* B33 DINV2*
8 BI H_STBP<3>* E25 HDSTBP3*
8 BI H_STBN<3>* D25 HDSTBN3*
8 BI H_DBI<3>* C26 DINV3*

8 BI H_ADS* T36 ADS*
8 BI H_TRDY* V30 HTRDY*
8 OUT H_DRDY* U36 DRDY*
8 OUT H_DEFER* N36 DEFER*
8 BI H_HITM* M36 HITM*
8 BI H_HIT* P36 HIT*
8 BI H_LOCK* T35 HLOCK*
9 8 OUT H_BR<0>* U33 BREQ0*
8 BI H_BNR* T34 BNR*
8 OUT H_BPRI* M34 BPRI*
8 BI H_DBSY* U31 DBSY*
0 R36 RS0*
8 OUT H_RS<2..0>* 1 U34 RS1*
2 P34 RS2*
9 IN H_CPURST* D22 CPURST*
E7 PWROK

DEBUG

69 52 IN PWRGD_3V
R6C22 1 2
0 603 1A CH
DEBUG ONLY

H_D<63..0>* BI 8

HD0* T30 0
HD1* R33 1
HD2* R34 2
HD3* N34 3
HD4* R31 4
HD5* L33 5
HD6* L36 6
HD7* P35 7
HD8* J36 8
HD9* K34 9
HD10* K36 10
HD11* M30 11
HD12* M35 12
HD13* L34 13
HD14* K35 14
HD15* H36 15
HD16* G34 16
HD17* G36 17
HD18* J33 18
HD19* D35 19
HD20* F36 20
HD21* F34 21
HD22* E36 22
HD23* H34 23
HD24* F35 24
HD25* D36 25
HD26* H35 26
HD27* E33 27
HD28* E34 28
HD29* B35 29
HD30* G31 30
HD31* C36 31
HD32* D33 32
HD33* D30 33
HD34* D29 34
HD35* E31 35
HD36* D32 36
HD37* C34 37
HD38* B34 38
HD39* D31 39
HD40* G29 40
HD41* C32 41
HD42* B31 42
HD43* B32 43
HD44* B30 44
HD45* B29 45
HD46* E27 46
HD47* C28 47
HD48* B27 48
HD49* D26 49
HD50* D28 50
HD51* B26 51
HD52* G27 52
HD53* H26 53
HD54* B25 54
HD55* C24 55
HD56* B23 56
HD57* B24 57
HD58* E23 58
HD59* C22 59
HD60* G25 60
HD61* B22 61
HD62* D24 62
HD63* G23 63

HD_VREF0 H30
HD_VREF1 H24
HD_VREF2 D27
HA_VREF AD30
HCC_VREF P30

GMCH_GTLREF IN 15

2 OF 5
IC

NB
C4E2 .1UF 10V 16V X7R 603
C4E1 .1UF 10V 16V X7R 603
C4D2 .1UF 10V 16V X7R 603
C4D1 .1UF 10V 16V X7R 603
C5D16 .1UF 10V 16V X7R 603

CAD NOTE:
DO NOT TEST POINT

66 IN V_1P5_CORE

NB
U6D1
BDG_DDR_2P0

AB10 VCCAGP
V10 VCCAGP
P10 VCCAGP
A7 VCCAGP
L1 VCCAGP
R9 VCCAGP
P6 VCCAGP
R1 VCCAGP
W9 VCCAGP
A3 VCCAGP
C1 VCCAGP
K6 VCCAGP
G1 VCCAGP
L9 VCCAGP
V6 VCCAGP
D6 VCCAGP
D4 VCCAGP

AC1 VCCHI
AC9 VCCHI
AD6 VCCHI
AE3 VCCHI

BG_VTTDECAP_AC37 AC37 VTTDECAP
BG_VTTDECAP_R37 R37 VTTDECAP
BG_VTTDECAP_L37 L37 VTTDECAP
BG_VTTDECAP_G37 G37 VTTDECAP
BG_VTTDECAP_A31 A31 VTTDECAP

K16 VCC
K14 VCC
K12 VCC
K10 VCC
A9 VCC
D10 VCC
H14 VCC
W20 VCC
A11 VCC
B9 VCC
B10 VCC
B11 VCC
B12 VCC
C9 VCC
C10 VCC
C11 VCC
C12 VCC
D9 VCC
D11 VCC
D12 VCC
E9 VCC
E11 VCC
F10 VCC
F12 VCC
G11 VCC
G13 VCC
H10 VCC
H12 VCC
J11 VCC
J13 VCC
J15 VCC
U17 VCC
U19 VCC
U21 VCC
V19 VCC
W17 VCC
W18 VCC
W19 VCC
W21 VCC
Y19 VCC
AA17 VCC
AA19 VCC
AA21 VCC

13 IN VCCA_DPLL A13 VCCA_DPLL
13 IN V_1P5_DAC A15 VCCA_DAC
B14 VCCA_DAC
13 IN V_1P5_VCCA_FSB A17 VCCA_FSB
66 IN V_1P5_CORE AD10 VCCA_HI
13 IN V_1P5_VCCA_SM AG2 VCCA_SM
AG1 VCCA_SM
13 IN V_2P5_VCCQ AT20 VCCQSM
AT21 VCCQSM
AU21 VCCQSM
3 OF 5
IC

VCCP IN 67 69

VTTFSB AD28
VTTFSB Y28
VTTFSB T28
VTTFSB M28
VTTFSB K26
VTTFSB K22
VTTFSB K20
VTTFSB K18
VTTFSB F18
VTTFSB B18
VTTFSB B19
VTTFSB B20
VTTFSB C18
VTTFSB C19
VTTFSB C20
VTTFSB D18
VTTFSB D19
VTTFSB D20
VTTFSB E19
VTTFSB F20
VTTFSB G19
VTTFSB H18
VTTFSB H20
VTTFSB J19

V_2P5_SM IN 58

VCCSM AH26
VCCSM AH22
VCCSM AH18
VCCSM AH14
VCCSM AH12
VCCSM AH10
VCCSM AJ1
VCCSM AK2
VCCSM AL5
VCCSM AU13
VCCSM AU17
VCCSM AU25
VCCSM AU29
VCCSM AU33
VCCSM AG7
VCCSM AG9
VCCSM AH2
VCCSM AH3
VCCSM AH4
VCCSM AH6
VCCSM AH8
VCCSM AJ2
VCCSM AJ3
VCCSM AJ4
VCCSM AJ5
VCCSM AJ7
VCCSM AJ9
VCCSM AJ11
VCCSM AJ15
VCCSM AJ19
VCCSM AJ23
VCCSM AK3
VCCSM AK4
VCCSM AK6
VCCSM AK8
VCCSM AK10
VCCSM AK32
VCCSM AL1
VCCSM AL2
VCCSM AL3
VCCSM AL4
VCCSM AL7
VCCSM AL9
VCCSM AL11
VCCSM AL37
VCCSM AM14
VCCSM AM18
VCCSM AM22
VCCSM AM26
VCCSM AU9
VCCSM AU5
VCCSM AP20
VCCSM AP15
VCCSM AP7
VCCSM AM30
VCCSM AJ27

VCCGPIO B6
VSSA_DAC B15
VSSA_DAC C14

VCC3

C6D2 .1UF 20V 25V X5R 603 NB

DRAWING
FAB_A.SCH.1.12
Mon Nov 18 13:48:37 2002
D845GFT FAB_A

[PAGE_TITLE=82845GV_CHIPSET]
PART 2 OF 3

DOCUMENT NUMBER	PAGE	REV
C23021	12	4.0

ROOM=DCL_CORE_GMCH

ALTERNATE PART# 721891-008

721891-009

66 IN V_1P5_CORE — R6D2 1.0 603 5% CH — L6D1 10UH IND — NB — VCCA_DPLL OUT 12

C5C6 470UF 20% 10V EMPTY RDL

C5C11 680UF 20% 10V ALUM RDL

C5D19 .1UF 10% 10V CERMTY 603

DFP

DEBUG ONLY DEBUG

66 IN V_1P5_CORE — R5D5 0 603 1A CH — V_1P5_DAC OUT 12

C5D20 .1UF 10% 10V X7R 603

C5D10 .01UF 10% 50V X7R 603

NB

ANALOG FILTERS

NB

202287-054

L5D1 .82UH IND

66 IN V_1P5_CORE — V_1P5_VCCA_FSB OUT 12

C5C7 22UF 20% 25V ELEC RDL

C5D9 .1UF 10% 16V X7R 603

L6E1 1UH IND

66 IN V_1P5_CORE — V_1P5_VCCA_SM OUT 12

C6E11 100UF 20% 25V ELEC RDL

C6E10 .1UF 10% 16V X7R 603

L5F1 .68UH IND

58 IN V_2P5_SM — V_2P5_VCCQ OUT 12

C5F7 4.7UF 10% 16V X5R 1206

C5F1 .1UF 10% 16V X7R 603

R5F1 1.0 5% CH 603

PILOT	BALL	FUNCTION	H	L
0	Y3	FSB SPEED	133	100
1	Y2	MEMORY TYPE	DDR	SDR
2	AA2	INT. GFX DIS	DISABLE	ENABLE
3	Y4	MEMORY SPEED	DDR 200	PC133 / DDR 266
4	AA3	RSVRD	?	?
5	AA5	RSVRD	?	?

VCC3_CLK IN 7

H_SEL133_100_JMPR OUT 7

R6C4 1.5K 5% CH 603

2R6C13 1A EMPTY 0 603

H_FSBSEL0 IN 8

R6C12 5% CH 8.2K 603

R6C16 8.2K 5% CH 603

HDR TH J6C2 102276-003

DEBUG ONLY DEBUG

DEFAULT 1-2

J6C2	SPEED
1-2	CPU SELECT
2-3	100MHZ
EMPTY	133MHZ

U6D1 BDG_DDR_2P0

76 OUT	TP_BG_RSVD_Y3	Y3	PSBSEL	
76 OUT	TP_BG_RSVD_Y2	Y2	MEMSEL	
75 OUT	TP_BG_RSVD_AA2	AA2	RSVD	
OUT	TP_BG_RSVD_AA4	AA4	RSVD	
OUT	TP_BG_RSVD_AA3	AA3	RSVD	
OUT	TP_BG_RSVD_AA5	AA5	RSVD	
OUT	TP_BG_RSVD_W7	W7	RSVD	
76 OUT	TP_BG_RSVD_Y4	Y4	RSVD	
OUT	TP_BG_RSVD_Y8	Y8	RSVD	
	TP_BG_RSVD_A37	A37	RSVD	

4 OF 5 IC

DDCA_DATA C7 — GLUE4_DDCSDA_3V B1 52 69

DDCA_CLK D7 — GLUE4_DDCSCL_3V B1 52 69

RED C15 — VGA_RED OUT 69 22

RED* D16 — VGA_RED* OUT 69 22

GREEN E15 — VGA_GREEN OUT 69 22

GREEN* F16 — VGA_GREEN* OUT 69 22

BLUE G15 — VGA_BLUE OUT 69 22

BLUE* H16 — VGA_BLUE* OUT 69 22

HSYNC B7 BG_HSYNC_B7

VSYNC C6 BG_VSYNC_C6

DREFCLK D14

REFSET B16

R5D6 137 1% CH 603

CR5D3 GP SOT23S DIO

CR5D1 GP SOT23S DIO

CR5D2 GP SOT23S DIO

201036-001

V_1P5_CORE IN 66

C5D3 .1UF 20% 25V Y5U 603

VIDEO

R6C192 47 5% CH 603

U6C2 74AHCT1G08

EMPTY VCC=5 GND=3

R6C18 0 603 1A CH

HSYNC_5V OUT 69 22

R6C202 47 5% CH 603

U6C1 74AHCT1G08

R6C17 0 603 1A CH

VSYNC_5V OUT 69 22

CR6C1 GP SOT23S EMPTY

CR6C2 GP SOT23S EMPTY

VCC3

CK_48M_DOTCLK IN 7

82845GV CHIPSET

PART 3 OF 3

[PAGE_TITLE= _CHIPSET_3_OF_3]

D845GFT FAB_A

DRAWING

FAB_A.SCH.1.13

Mon Nov 18 13:48:47 2002

DOCUMENT NUMBER	PAGE	REV
C23021	13	4.0

INTENTIONALLY LEFT BLANK

DRAWING

FAB_A.SCH.1.14
Mon Nov 25 12:48:57 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	14	4.0

ROOM=DCL_CORE_GMCH

SYSTEM MEMORY DECOUPLING

EMPTY FOR ITTO

58 IN V_2P5_MEM

C6F1 100UF 20% 25V ELEC RDL

C6F2 .1UF 10% 16V X7R 603

C4F1 .1UF 10% 16V X7R 603

C5F6 .1UF 10% 16V X7R 603

C4E3 .1UF 10% 16V X7R 603

C5F5 .1UF 10% 16V X7R 603

C5F3 .1UF 10% 16V X7R 603

C5F2 .1UF 10% 16V X7R 603

C5F4 .1UF 10% 16V X7R 603

MEM_DCPL MEM_DCPL MEM_DCPL MEM_DCPL MEM_DCPL MEM_DCPL MEM_DCPL MEM_DCPL

66 IN V_1P5_CORE

C6D1 100UF 20% 25V ELEC RDL

C6D4 4.7UF 20% EMPTY 1206

C5D8 4.7UF 20% EMPTY 1206

C5D14 .1UF 10% 16V X7R 603

C6E7 .1UF 10% 16V X7R 603

C6E6 .1UF 10% 16V X7R 603

C5D13 .1UF 10% 16V X7R 603

C6D5 .1UF 10% 16V EMPTY 603

C6D7 .1UF 10% 16V X7R 603

C6D6 .1UF 10% 16V X7R 603

C6E3 .1UF 10% 16V X7R 603

C6E1 .1UF 10% 16V X7R 603

C6D3 220UF 20% 25V TANT ELEC RDL

NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL

69 67 IN VCCP

C5D1 1UF 10% 16V X7R 603

C5D18 1UF 10% 16V X7R 603

C5D15 1UF 10% 16V X7R 603

C5D7 1UF 10% 16V EMPTY 603

C5D12 1UF 10% 16V X7R 603

C5D11 1UF 10% 16V X7R 603

C5D17 1UF 10% 16V X7R 603

NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL NB_DCPL

C5D5 10.0UF 20% 6.3V X5R 1206

C5D4 10.0UF 20% 6.3V X5R 1206

NB_DCPL NB_DCPL

CAPS FOR PSB GENERIC

CAD NOTE:

HYSWING VOLTAGE "10MIL TRACE, 7MIL SPACE"
DESIGN NOTE: HYSWING S/B 1/3*VCCP +/- 2%

69 67 IN VCCP

R5D1 301 1% CH 603

C5D2 .01UF 10% 50V X7R 603

HYSWING OUT 12

R5T1 0 1A EMPTY 603

CUT TRACE BETWEEN RESISTOR PADS OF R5T1 FOR MARGINING ON 6 LAYER BOARD

I91

HXSWING OUT 12

R5D3 150 1% CH 603

NOTE: HXSWING

69 67 IN VCCP

202286-068 R5D2 49.9 603 1% CH

GMCH_GTLREF OUT 12 77

C5D6 .1UF 10% 16V X7R 603

R5D4 100 1% CH 603

CAP FOR GTLREF INPUTS @GMCH
USE 12MIL TRACE, ISOLATE W/ 10MIL SPACE
CAP SHOULD BE PLACED NEAR GMCH PIN

66 IN V_1P5_CORE

R6E6 68.1 1% CH 603

HI_RCOMP_GMCH OUT 11

GRCOMP OUT 11

HYRCOMP OUT 12

HXRCOMP OUT 12

R6D5 40.2 1% CH 603

R4E1 24.9 1% CH 603

R5D7 24.9 1% CH 603

NB NB NB

DESIGN NOTES:

VSWING S/B 0.466*VDD (1.5V) +/- 2%
HUBREF S/B 0.233*VDD (1.5V) +/- 2%

PLACEMENT NOTES:
RESISTOR DIVIDER PLUS 1 CAP PLACED AT MIDPOINT OF BUS. TWO OTHER CAPS PLACED 1 EA AT GMCH AND ICH
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE

66 IN V_1P5_CORE

R7F9 226 1% CH 603

R6F4 100 1% CH 603

C6F5 1UF 10% 16V X7R 603

R6F3 100 1% CH 603

C6F4 1UF 10% 16V X7R 603

R7F14 0 603 1A CH

NOTE: DEBUG ONLY

R7F12 0 603 1A CH

NOTE: DEBUG ONLY

HI_VSWING_GMCH OUT 69 11

HI_VSWING_ICH OUT 24

C6E8 .01UF 10% 50V X7R 603

C7F8 .01UF 10% 50V X7R 603

HI_VREF_GMCH OUT 69 11 76

HI_VREF_ICH OUT 24

C6F9 .01UF 10% 50V X7R 603

C7F6 .01UF 10% 50V X7R 603

CHIPSET DECOUPLING, STRAPPING

DRAWING
FAB_A.SCH.1.15
Mon Nov 18 13:48:55 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	15	4.0

DDR SERIES RESISTORS

ROOM=DCL_DDR_CORE

M_DQS_RS<7..0> OUT 17 18

M_DM_RS<7..0> BI 17 18

M_DQ_RS<63..0> BI 17 18

11 IN M_DQS<7..0>

11 BI M_DM<7..0>

11 BI M_DQ<63..0>

R2F8 7 1 2 7 10 5% CH
R2F10 6 1 2 6 10 5% CH
R3F4 5 1 2 5 10 5% CH
R3F1 4 1 2 4 10 5% CH
R4F1 3 1 2 3 10 5% CH
R5F4 2 1 2 2 10 5% CH
R5F2 1 1 2 1 10 5% CH
R6F7 0 1 2 0 10 5% CH

R2F7 7 1 2 7 10 5% CH
R2F9 6 1 2 6 10 5% CH
R3F3 5 1 2 5 10 5% CH
R3F2 4 1 2 4 10 5% CH
R4F2 3 1 2 3 10 5% CH
R5F5 2 1 2 2 10 5% CH
R5F3 1 1 2 1 10 5% CH
R6F8 0 1 2 0 10 5% CH

RP2F2 63 2 7 63 10 5% IC
RP2F2 62 4 5 62 10 5% IC
RP2F3 61 2 7 61 10 5% IC
RP2F3 60 4 5 60 10 5% IC
RP2F2 59 1 8 59 10 5% IC
RP2F2 58 3 6 58 10 5% IC
RP2F3 57 1 8 57 10 5% IC
RP2F3 56 3 6 56 10 5% IC
RP2F1 55 3 6 55 10 5% IC
RP2F1 54 4 5 54 10 5% IC
RP2F4 53 1 8 53 10 5% IC
RP2F4 52 2 7 52 10 5% IC
RP2F1 51 1 8 51 10 5% IC
RP2F1 50 2 7 50 10 5% IC
RP2F4 49 3 6 49 10 5% IC
RP2F4 48 4 5 48 10 5% IC

RP2F5 47 1 8 47 10 5% IC
RP2F5 46 3 6 46 10 5% IC
RP3F3 45 2 7 45 10 5% IC
RP3F3 44 3 6 44 10 5% IC
RP2F5 43 2 7 43 10 5% IC
RP2F5 42 4 5 42 10 5% IC
RP3F3 41 1 8 41 10 5% IC
RP3F3 40 4 5 40 10 5% IC
RP3F2 39 2 7 39 10 5% IC
RP3F2 38 3 6 38 10 5% IC
RP3F1 37 1 8 37 10 5% IC
RP3F1 36 3 6 36 10 5% IC
RP3F2 35 1 8 35 10 5% IC
RP3F2 34 4 5 34 10 5% IC
RP3F1 33 2 7 33 10 5% IC
RP3F1 32 4 5 32 10 5% IC

RP4F1 31 1 8 31 10 5% IC
RP4F1 30 3 6 30 10 5% IC
RP4F2 29 2 7 29 10 5% IC
RP4F2 28 3 6 28 10 5% IC
RP4F1 27 2 7 27 10 5% IC
RP4F1 26 4 5 26 10 5% IC
RP4F2 25 1 8 25 10 5% IC
RP4F2 24 4 5 24 10 5% IC
RP5F4 23 1 8 23 10 5% IC
RP5F4 22 3 6 22 10 5% IC
RP5F3 21 1 8 21 10 5% IC
RP5F3 20 4 5 20 10 5% IC
RP5F4 19 2 7 19 10 5% IC
RP5F4 18 4 5 18 10 5% IC
RP5F3 17 2 7 17 10 5% IC
RP5F3 16 3 6 16 10 5% IC

RP5F2 15 3 5 15 10 5% IC
RP5F2 14 4 5 14 10 5% IC
RP5F1 13 1 8 13 10 5% IC
RP5F1 12 2 7 12 10 5% IC
RP5F2 11 1 8 11 10 5% IC
RP5F2 10 2 7 10 10 5% IC
RP5F1 9 3 6 9 10 5% IC
RP5F1 8 4 5 8 10 5% IC
RP6F2 7 2 7 7 10 5% IC
RP6F2 6 3 6 6 10 5% IC
RP6F1 5 2 7 5 10 5% IC
RP6F1 4 3 6 4 10 5% IC
RP6F2 3 1 8 3 10 5% IC
RP6F2 2 4 5 2 10 5% IC
RP6F1 1 1 8 1 10 5% IC
RP6F1 0 4 5 0 10 5% IC

DRAWING
FAB_A.SCH.1.16
Mon Nov 18 12:43:47 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	16	4.0

ROOM=DCL_DDR_CORE

DDR DIMM 0

PRIMARY A13373-002
ALTERNATE A13373-001

J6G1
DIMM2P_184_CK

M_DQ_RS<63..0>
M_WE*
M_RAS*
M_CAS*
M_MAA<12..0>
M_MAA_CPC<5..1>
M_DM_RS<7..0>
M_DQS_RS<7..0>
M_SCS<3..0>*
M_SCKE<3..0>
M_BS<1..0>
SMB_DATA_ISO
SMB_CLK_ISO

CK_M_100_133M_P_DDR0
CK_M_100_133M_N_DDR0
CK_M_100_133M_P_DDR1
CK_M_100_133M_N_DDR1
CK_M_100_133M_P_DDR2
CK_M_100_133M_N_DDR2

V_2P5_SM
V_2P5_CORE
DIMM_VREF_1P25

R6F5 49.9 1% CH 603
R6F9 49.9 1% CH 603
PLACE RES DIVIDER NEAR DIMMS

C6G1 .1UF 10V X5R 603 NEAR DIMM PIN

DDR DIMM 1

PRIMARY A13373-002
ALTERNATE A13373-001

J6G2
DIMM2P_184_CK

M_DQ_RS<63..0>
M_WE*
M_RAS*
M_CAS*
M_MAA<12..0>
M_MAB_CPC<5..1>
M_DM_RS<7..0>
M_DQS_RS<7..0>
M_SCS<3..0>*
M_SCKE<3..0>
M_BS<1..0>
V_2P5_SM

CK_M_100_133M_P_DDR3
CK_M_100_133M_N_DDR3
CK_M_100_133M_P_DDR4
CK_M_100_133M_N_DDR4
CK_M_100_133M_P_DDR5
CK_M_100_133M_N_DDR5

V_2P5_SM
V_2P5_CORE
DIMM_VREF_1P25
SMB_CLK_ISO
SMB_DATA_ISO

C6F6 .1UF 10V X5R 603 NEAR DIMM PIN

DRAWING FAB_A.SCH.1.17
Mon Nov 18 13:49:05 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	17	4.0

ROOM=DCL_DDR_CORE

DDR TERMINATION RESISTORS

59 IN V_1P25_MEMVTT

17 16 IN M_DQS_RS<7..0>

17 16 BI M_DM_RS<7..0>

17 16 BI M_DQ_RS<63..0>

17 11 BI M_MAA<12..0>

RP2G5 RP2G3 R2G2 R3G1 RP4G5 RP5G7 RP5G2 RP6G2

RP6G2 RP5G2 RP5G7 R4G3 RP3G2 R2G1 RP2G3 RP2G5

RP1G1 RP2G5 RP2G4 RP1G1 RP1G1 RP2G5 RP2G4 RP2G3 RP2G4 RP2G3 RP2G2 RP2G2 RP2G4 RP2G4 RP2G2 RP2G2

RP2G1 RP2G1 RP3G3 RP3G3 RP2G1 R3G3 RP3G3 RP3G2 RP3G2 RP3G1 RP3G3 RP3G2 RP3G1 RP3G1

RP4G2 RP4G2 RP4G5 RP4G2 RP4G2 RP4G5 RP4G1 RP5G7 RP5G5 RP4G1 RP5G5 RP5G5

RP5G3 RP5G3 RP5G2 RP5G2 RP5G3 RP5G3 RP5G1 RP5G1 RP6G2 RP6G1 RP6G1 RP5G1 RP5G1 RP6G1

R5G1 RP5G6 RP4G4 RP5G6 RP5G6 RP5G6 R4G5 R4G4 RP4G4

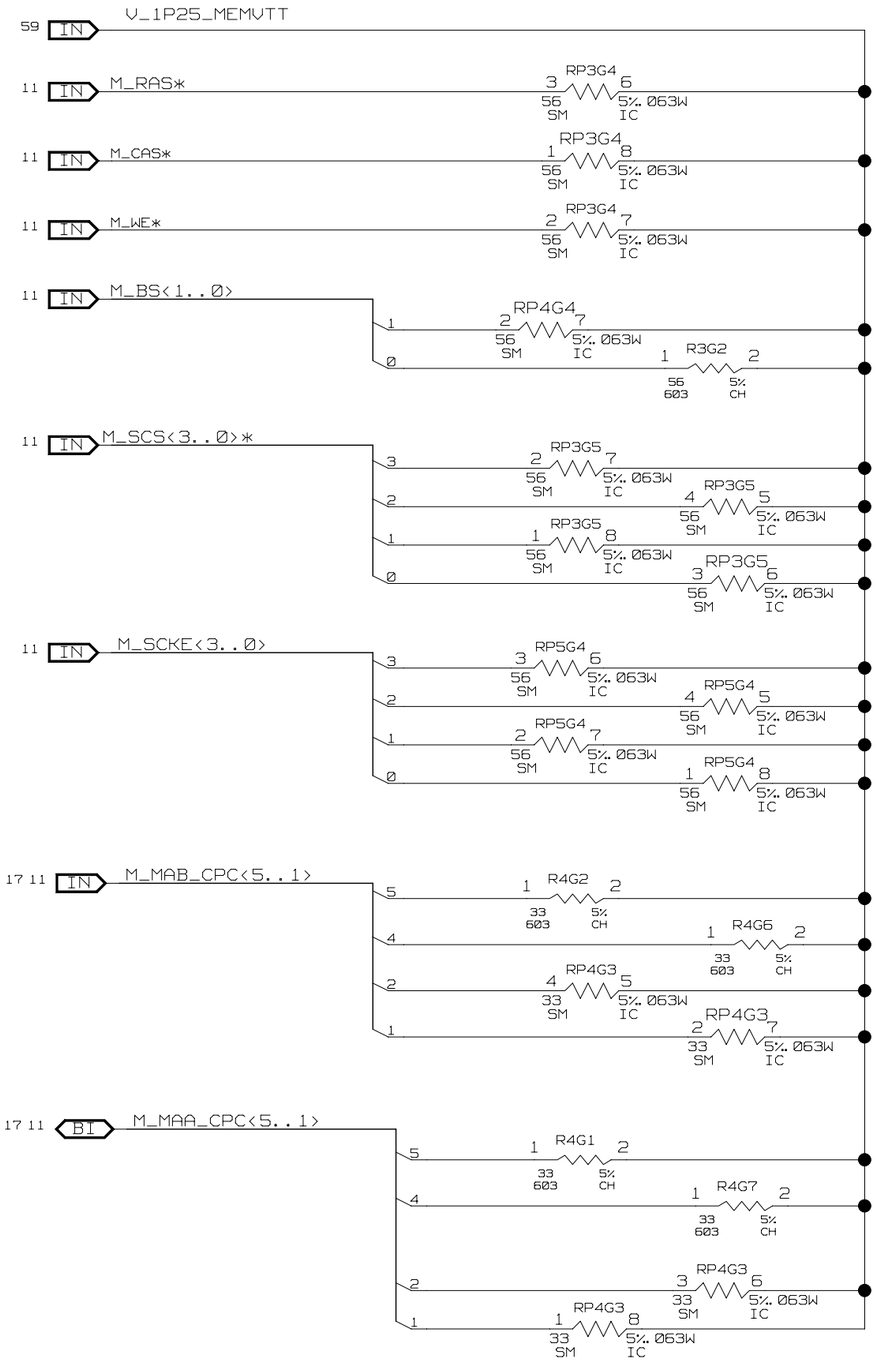
All resistors: 56 SM IC 5% .063W, except R2G2 56 603 CH 5%, R3G1 56 603 CH 5%, R4G3 56 603 CH 5%, R2G1 56 603 CH 5%, R3G3 56 603 CH 5%, R5G1 56 603 CH 5%, R4G5 56 603 CH 5%, R4G4 56 603 CH 5%

[PAGE_TITLE=DDR_TERMINATION_RESISTORS]

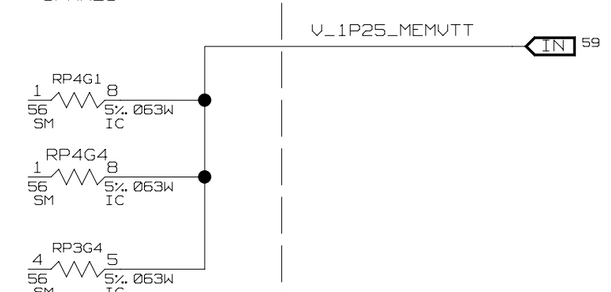
DRAWING FAB_A.SCH.1.18
Mon Nov 18 12:44:14 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	18	4.0

DDR TERMINATION RESISTORS



SPARES



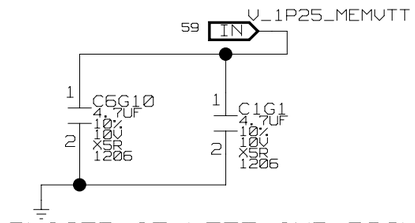
NOTE:

CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

DRAWING
FAB_A.SCH.1.19
Mon Nov 18 12:44:23 2002
D845GFT FAB_A

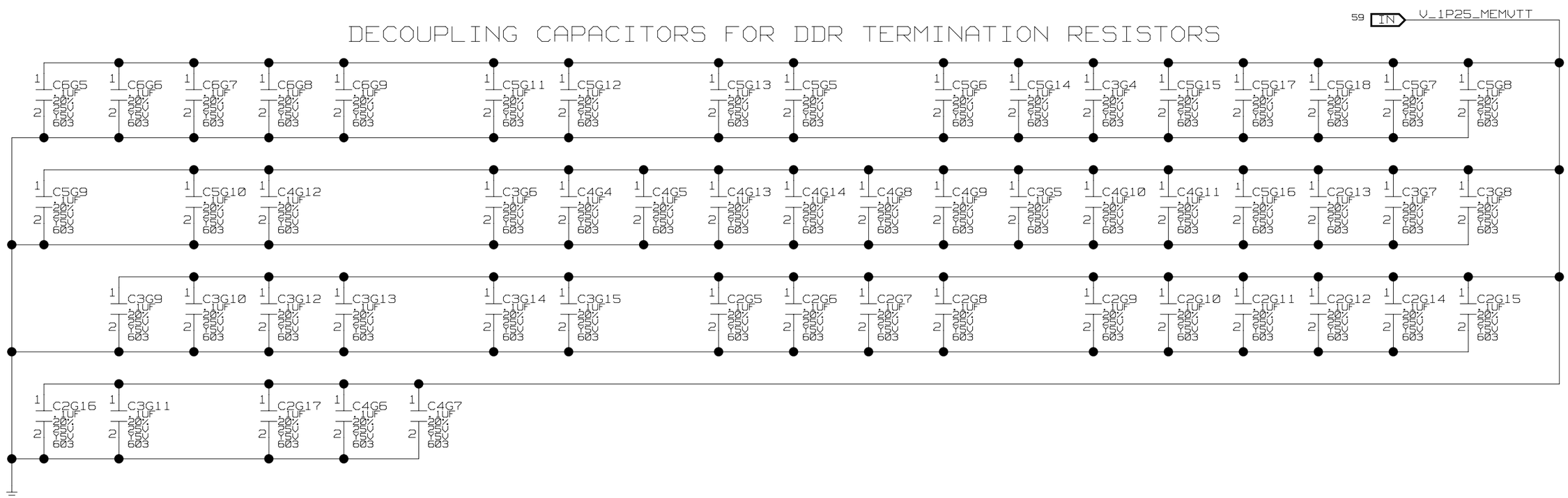
DOCUMENT NUMBER	PAGE	REV
C23021	19	4.0

[FULL_ID=1164-20-16428] [PAGE_INFO_ID=16428] [MODULE_ID=1130-19-15164] [DONOR_ID=1130-19-15164]



PLACED AT LEFT AND RIGHT ENDS
OF VTT ISLAND

DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS



DRAWING
FAB_A.SCH.1.20
Mon Nov 18 14:44:58 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	20	4.0

[FULL_ID=1164-21-16430] [PAGE_INFO_ID=16430] [MODULE_ID=1130-13-15152] [DONOR_ID=1130-13-15152]

ROOM=DCL_CORE_AGP

OPTION TO STUFF AT ALTERED ASSEMBLY LEVEL

RM6C1
AGP RETENTION MECH
A16226-001

66 IN V_1P5_CORE

EMPTY
RP7C2 6.80K 5% .063W EMPTY SM
RP7C3 6.80K 5% .063W EMPTY SM
RP7C2 6.80K 5% .063W EMPTY SM

11 IN G_ST<2..0>

11 BI G_AD<31..0>

J5C1
DEBUG CONN

ST2		
ST1		
ST0		
GAD31	GDEVSEL	G_DEVSEL* BI 11
GAD30	GTRDY	G_TRDY* BI 11
GAD29	GIRDY	G_IRDY* BI 11
GAD28	GFRAME	G_FRAME* BI 11
GAD27	GSTOP	G_STOP* BI 11
GAD26	GPERR	G_PERR_R*
GAD25	GSERR	G_SERR_R*
GAD24	GPAR	G_PAR BI 11
GAD23	WBF	G_WBF* OUT 11
GAD22	GREQ	G_REQ* OUT 11
GAD21	GGNT	G_GNT* IN 11
GAD20	RBF	G_RBF* OUT 11
GAD19	PIPE	G_PIPE* OUT 11
GAD18	12V	+12V
GAD17	VCC	+VCC
GAD16	VCC	
GAD15	VCC3	+VCC3
GAD14	VCC3	
GAD13	VCC3	
GAD12	VCC3	
GAD11	VCC3	
GAD10	VCC3	
GAD9	VCC3	
GAD8	VCC3	
GAD7	VDDQ	V_1P5_CORE IN 66
GAD6	VDDQ	
GAD5	VDDQ	
GAD4	VDDQ	
GAD3	VDDQ	
GAD2	VDDQ	
GAD1	VDDQ	
GAD0	VDDQ	
GAD_STB0	VDDQ	
GAD_STB1	VDDQ	
GAD_STB0	SBA7	G_SBA<7..0> OUT 11
GAD_STB1	SBA6	
SB_STB	SBA5	
SB_STB	SBA4	
GC_BE3	SBA3	
GC_BE2	SBA2	
GC_BE1	SBA1	
GC_BE0	SBA0	
USB+	3.3VAUX	V_3P3_PCIVAUX IN 61 69 72
USB-	VREFGC	TP_AGP_VREFGC_A66
INTA	VREFCG	
INTB	RSVD	TP_AGP_1P5_A3
AGPCLK	RSVD	TP_AGP_1P5_A11
PCIRST	RSVD	TP_AGP_1P5_B14
OVRCNT	RSVD	TP_AGP_1P5_A22
TYPEDET	RSVD	TP_AGP_1P5_B22
PME	RSVD	TP_AGP_1P5_A24

CONN

TP_USB_PLUS
TP_USB_MINUS
TP_OVRCNT*
TP_TYPEDET*

66 IN V_1P5_CORE
CHECK PULL-UP VALUES PER AGP2.0
RP7D1 6.80K 5% .063W EMPTY SM
RP7C2 6.80K 5% .063W EMPTY SM
RP7C3 6.80K 5% .063W EMPTY SM
R7E3 6.8K 5% CH 603
R7E2 6.8K 5% CH 603
R7E1 6.8K 5% EMPTY 603
R7E4 6.8K 5% EMPTY 603
PLACE ON CHIPSET SIDE OF AGP CONN

R7E5 330 5% EMPTY 603
NOTE:
DVO SUPPORT

CAD PLACEMENT NOTE:
ENSURE STUB LENGTH TO RESN. IS < 100MIL

::REMOVE ON FAB_B::
PLACE ON CHIPSET SIDE OF AGP CONN

66 IN V_1P5_CORE
R6C21 6.8K 5% EMPTY 603
R6D3 6.8K 5% EMPTY 603
R6E7 6.8K 5% EMPTY 603

11 BI G_ADSTB0
11 BI G_ADSTB1
11 BI G_ADSTB0*
11 BI G_ADSTB1*
11 BI G_SBSTB
11 OUT G_SBSTB*
11 BI G_C_BE<3..0>*

R6D1 6.8K EMPTY 603
R6D4 6.8K EMPTY 603
R6E8 6.8K EMPTY 603

23 69 34 31 BI P_INTA*
23 69 34 31 BI P_INTB*
7 IN CK_G_66M_AGP
33 32 31 69 52 BI P_RST_SLOTS*
23 69 33 32 31 BI P_PME*

NC=1,2,3
GND=A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A37, B37, A49, B49, A55, B55, A61, B61

66 IN V_1P5_CORE
R6E10 1K 1% 603 CH
AGPREF_GMCH OUT 11
R6E9 1K 1% 603 CH
C6E4 1UF 10% 16V X7R 603 PLACE NEAR GMCH

DESIGN NOTE:
TO AGP CONNECTOR
10 uA LOAD
R6F1 0 1A 603 CH
CAD NOTE:
PLACE NEAR GMCH PINS
AGPREF_CON
C7F3 1UF 10% 16V X7R 603 PLACE NEAR AGP

CAD PLACEMENT NOTE:
PLACE RESISTORS NEAR AGP CONN

VCC3 AGP_DCPL C7D6 100UF 20% 25V TANT ELEC RDL
VCC3 AGP_DCPL C7C10 22UF 20% 25V TANT ELEC RDL
VCC AGP_DCPL C6CB 22UF 20% 25V ELEC RDL

VCC3
+12V AGP_DCPL C6C9 1UF 20% 50VC X7R 603
VCC AGP_DCPL C6C7 1UF 20% 10VC X7R 603
AGP_DCPL C6C12 1UF 20% 25VC X7R 603
AGP_DCPL C7D5 1UF 20% 25VC X7R 603
AGP_DCPL C7D1 1UF 20% 25VC X7R 603

66 IN V_1P5_CORE
AGP_DCPL C6E2 100UF 20% 25V TANT ELEC RDL
AGP_DCPL C7D7 1UF 20% 25VC X7R 603
AGP_DCPL C7E4 1UF 20% 25VC X7R 603
AGP_DCPL C6E5 1UF 20% 25VC X7R 603
AGP_DCPL C6E12 1UF 20% 25VC X7R 603
AGP_DCPL C7E2 1UF 20% 25VC X7R 603
AGP_DCPL C7D9 1UF 20% 25VC X7R 603
CAD NOTE:
PLACE NEAR AGPCONN

DRAWING
FAB_A.SCH.1.21
Mon Nov 18 12:44:33 2002
D845GET FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	21	4.0

COMPONENTS ARE DFM29

69 13 IN VGA_RED
69 13 IN VGA_RED*
69 13 IN VGA_GREEN
69 13 IN VGA_GREEN*
69 13 IN VGA_BLUE
69 13 IN VGA_BLUE*
69 13 IN HSYNC_5V
69 13 IN VSYNC_5V

VCC
-3 DB @ 100MHZ
RT4A1 THRMSTR
VDO_J0401G_RC
R4A4 2 0 805 1A CH
C4A15 1UF 20% 25V Z5U 603

75 OHM @ 100MHZ 200 MA
FB4A1 FB
75 OHM @ 100MHZ 200 MA
FB5A2 FB
75 OHM @ 100MHZ 200 MA
FB5A1 FB

J4A1 RCPT
VDO_RED_L
VDO_J0401G_9
VDO_GREEN_L
VDO_BLUE_L
TP_VDOCONN_11_CORE
TP_VDOCONN_4_CORE

R4A1 75 1% CH 603
C4A4 .30PF 50V Z5U 603
C4A3 .30PF 50V Z5U 603
R5A5 75 1% CH 603
C5A5 .30PF 50V Z5U 603
C4A2 .30PF 50V Z5U 603
R5A3 75 1% CH 603
C5A3 .30PF 50V Z5U 603
C4A1 .30PF 50V Z5U 603

CP4A1 470PF 20% 50V X7R SM
CP4A1 470PF 20% 50V X7R SM

C4A5 20PF 10% 50V X7R 603
R4A2 37.4 1% CH 603
C5A2 20PF 10% 50V X7R 603
R5A2 37.4 1% CH 603
C5A4 20PF 10% 50V X7R 603
R5A4 37.4 1% CH 603

COMP PINS WANT RESISTOR CLOSEST TO 37.5 OHMS 1%

ROUTE AS CLOSE AS POSSIBLE TO 75 OHM RESISTORS

VCC
RP4J2 2.2K 5% .063W IC SM
RP4J2 2.2K 5% .063W IC SM

52 BI GLUE4_DDCSDA_5V
R5J2 100 5% 603 CH
VDO_MONID1_R
R5J3 100 5% 603 EMPTY DEBUG ONLY
R5J4 100 5% 603 EMPTY
52 BI GLUE4_DDCSCL_5V
R5J1 100 5% 603 CH
VDO_MONID2_R

I259 CR4B1 TVS6_2V 6.2V EMPTY

CP4A1 470PF 20% 50V X7R SM
CP4A1 470PF 20% 50V X7R SM

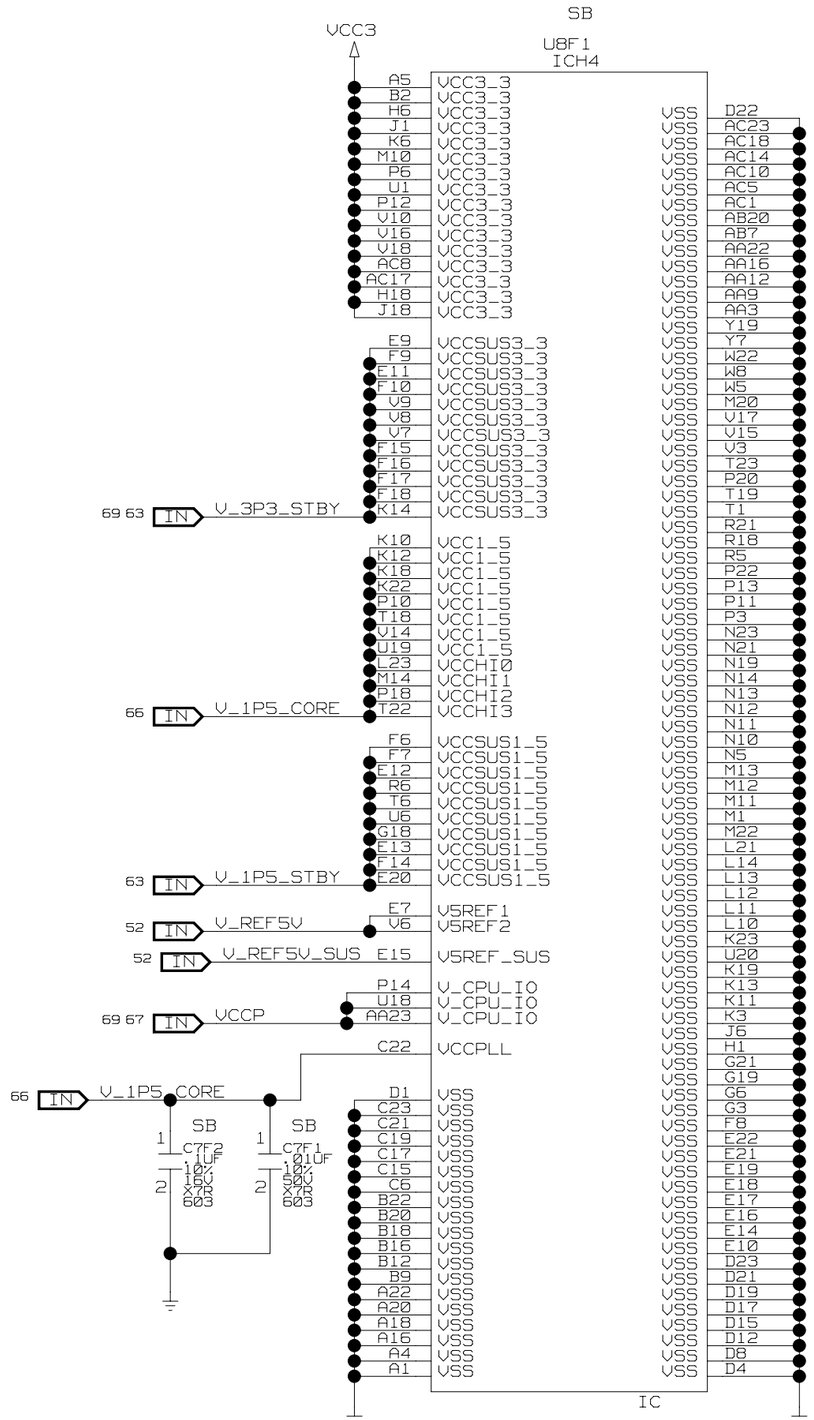
SPARES
RP4J2 2.2K 5% .063W IC SM
RP4J2 2.2K 5% .063W IC SM

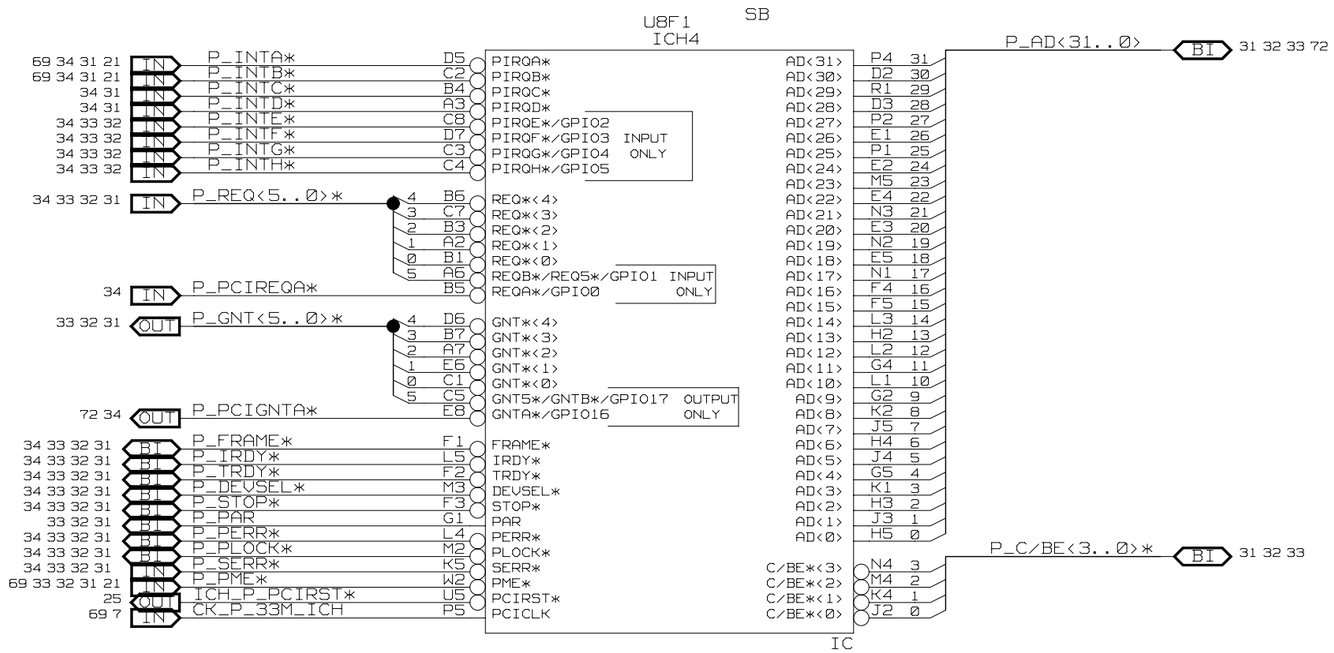
VGA CONNECTOR

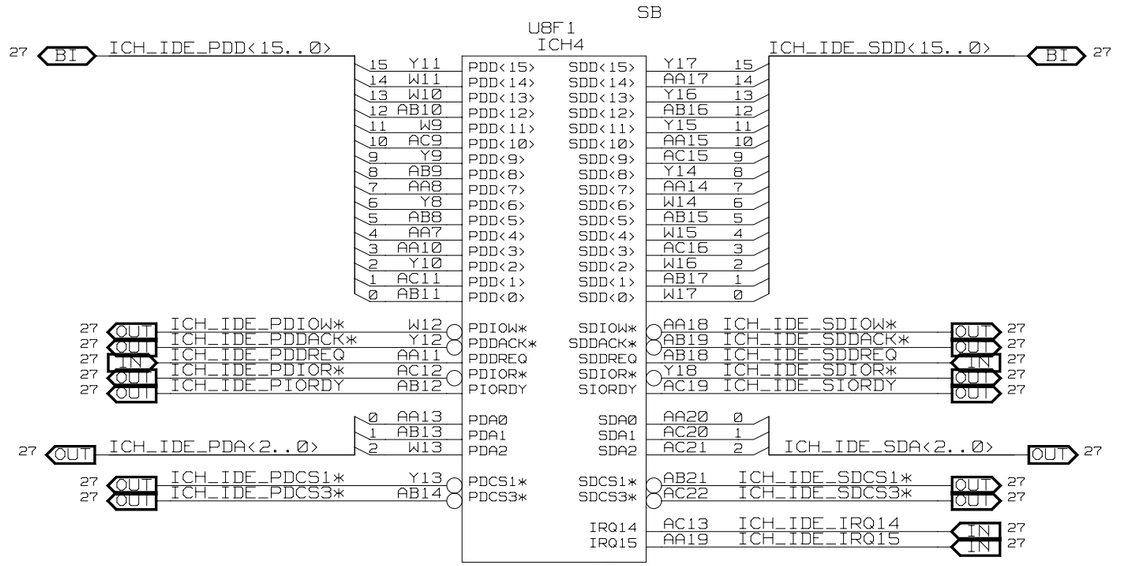
[PAGE_TITLE=VGA_CONNECTOR]

DRAWING
FAB_A.SCH.1.22
Mon Nov 18 12:44:43 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	22	4.0







[PAGE_TITLE=ICH4_A]

DRAWING
FAB_A.SCH.1.23
Mon Nov 18 13:49:26 2002
D845GFT FAB_A

CPU/AC97/SYS_MGMT

	DOCUMENT NUMBER	PAGE	REV
	C23021	23	4.0

DEBUG

SB

U8F1
ICH4

25 IN APICD0_1
8 77 69 OUT H_STPCLK*
77 OUT ICH_H_STPCLK*
8 69 OUT H_A20M*
8 69 OUT H_SLP*
8 69 9 OUT H_PWRGD
8 69 OUT H_INTR
8 69 OUT H_NMI
76 8 77 69 OUT H_SMI*
77 OUT ICH_H_SMI*
8 69 OUT H_IGNNE*
46 IN A20GATE
46 IN KBRST*
69 9 8 IN H_FERR*
51 8 69 OUT H_INIT*
72 46 BI SER_IRQ
75 51 46 OUT L_FRAME*
46 IN L_DRQ*
75 51 46 BI L_AD<3..0>
46 OUT SUSCLK
25 OUT INTRUDER*
25 IN ICH_RTCRST
69 52 IN PWRGD_3V
52 IN ICH_RSMRST*
61 IN V_3P0_BAT_VREG
25 IN ICH_VBIAS
25 IN ICH_RTCX1
25 IN ICH_RTCX2

#1 1 R3H6 2 0 603 1A CH
R7G4 R7F15 R7F16 R7F17 R7G3 R7F18 R7F1 RP7F1 SB
#1 1 R2H4 2 DEBUG 0 603 1A CH

J19	APICCLK	GPIO06	R2
H19	APICD_0	GPIO07	R3
K20	APICD_1	GPIO08	V4
V23	STPCLK*	GPIO12	V5
AB23	A20M*	GPIO13	W3
U21	CPUSLP*		
Y23	CPUPWRGD	GPIO18	Y21
AB22	INTR	GPIO19	W18
V21	NMI	GPIO20	W19
W23	SMI*	GPIO21	T3
W21	IGNNE*	GPIO22	Y20
Y22	A20GATE	GPIO23	J21
U22	RCIN*	GPIO24	AC2
AA21	FERR*	GPIO25	V2
V22	INIT*	GPIO27	W1
J22	SERIRQ	GPIO28	W4
T5	LFRAME*/FWH4	SLP_S3*	Y4
U3	LDRQ0*	SLP_S4*	Y2
U4	LDRQ1*	SLP_S5*	AA2
T2	LAD0/FWH0	RI*	Y1
R4	LAD1/FWH1	PWRBTN*	AA1
T4	LAD2/FWH2	SYS_RST*	Y3
U2	LAD3/FWH3	LANRST*	Y5
AA4	SUSCLK	TP0	AB2
W6	INTRUDER*	SUS_STAT*/LPCPD	AB3
W7	RTCRST*	VRMPWRGD	V19
AB6	PWROK	THERMTRIP*	W20
AA6	RSMRST*	THRM*	V1
AB5	VCCRTC	SMILINK0	AC3
Y6	VBIAS	SMLINK1	AB1
AC7	RTCX1	SMBDATA	AB4
AC6	RTCX2	SMBCLK	AC4
V20	NC	SMBALERT*/GPIO11	AA5
U23	NC	SPKR	H23
		CLK14	J23

INPUT ONLY / OUTPUT ONLY / I/O

TP_ICH_LDRQ1_U4
TP_GPIO_NO_POP*
TP_ICH_GPIO34
TP_ICH_GPIO35
TP_ICH_GPIO36
TP_ICH_GPIO41
TP_ICH_GPIO42

ICH_GPIO06_GPIO7 IN 25
ICH_GPIO8 IN 25
IO_SMI* IN 46
IO_PME* IN 46
TP_ICH_GP18
TP_ICH_GP19
TP_ICH_GP20
GPIO21_ISA_NOGO OUT 72
TP_ICH_GPIO22
TP_ICH_GPIO23
TP_ICH_GPIO24
GPIO_GRN_BLNK OUT 52
GPIO_YLW_BLNK OUT 52
GPIO_LAN_DISABLE* OUT 24 37
SLP_S3* OUT 52
SLP_S4* OUT 52
TP_SLP_S5*
ICH_RI_PU IN 25
SW_ON* IN 55
SYS_RST* IN 24
GPIO_LAN_DISABLE* IN 25
ICH_TP0_PU IN 25
SUS_STAT_PU* OUT 25
ICH_VRMPWRGD_PU IN 25
H_THERMTRIP_ICH* IN 9 69
ICH_THRM_PU* IN 25
SMB_DATA_MAIN BI 31 32 33 35 53 76
SMB_CLK_MAIN BI 31 32 33 35 53 76
SMB_ALERT_PU IN 25
SPKR OUT 38 54
CK_14M_ICH IN 7 69

V_3P3_STBY IN 63 69
R8F2 22K 5% CH 603 SB
R8F1 0 603 1A CH SB
FP_RST* IN 53 55 74

IC

SB U8F1 ICH4

C20	USBP_0	HI<0>	L19
D20	USBP_0*	HI<1>	L20
A21	USBP_1	HI<2>	M19
B21	USBP_1*	HI<3>	M21
C18	USBP_2	HI<4>	P19
D18	USBP_2*	HI<5>	R19
A19	USBP_3	HI<6>	T20
B19	USBP_3*	HI<7>	R20
C16	USBP_4	HI<8>	P23
D16	USBP_4*	HI<9>	L22
A17	USBP_5	HI<10>	N22
B17	USBP_5*	HI<11>	K21
B15	OC*<0>	HI_STBS	P21
C14	OC*<1>	HI_STBF	N20
A15	OC*<2>	HICOMP	R23
B14	OC*<3>	HISWING	R22
A14	OC*<4>	HIREF	M23
D14	OC*<5>	CLK66	T21
J20	GPIO32	LANRXD0	A10
G22	GPIO33	LANRXD1	A9
F20	GPIO34	LANRXD2	A11
G20	GPIO35	LANTXD0	B10
F21	GPIO36	LANTXD1	C10
H20	GPIO37	LANTXD2	A12
F23	GPIO38	LANRSTSYNC	B11
H22	GPIO39	LANCLK	C11
G23	GPIO40	EE_DIN	D11
H21	GPIO41	EE_CS	D10
F22	GPIO42	EE_SHCLK	C12
E23	GPIO43	EE_DOUT	A8
F19	CLK48	ACSYNC	C9
B23	USBRBIAS*	ACSDOUT	D9
A23	USBRBIAS	ACBITCLK	B8
		ACRST*	C13
		ACSDIN0	D13
		ACSDIN1	A13
		ACSDIN2	B13

I/O

USB_BPL_P0 BI 29 28
USB_BPL_P0* BI 29 28
USB_ICH_P1 BI 29
USB_ICH_P1* BI 29
USB_BPL_P2 BI 29 28
USB_BPL_P2* BI 29 28
USB_FP_P3 BI 30
USB_FP_P3* BI 30
USB_BPR_P4 BI 29 28
USB_BPR_P4* BI 29 28
USB_FP_P5 BI 30
USB_FP_P5* BI 30
USB_ICH_BPL_OC* IN 52
USB_ICH_CNR_OC* IN 30 29
USB_ICH_FP_OC* IN 30
USB_ICH_BPR_OC* IN 62
GPO_AUD_EN* OUT 36
BOARDID<3..0> BI 25
CDC_DWN_ENAB* OUT 36
CK_48M_ICH_USB IN 69 7

HI<10..0> BI 11 69 76
HI<11> BI 25
HI_STBS BI 11 69 76
HI_STBF BI 11 69 76
HI_RCOMP_ICH BI 25
HI_VSWING_ICH IN 15
HI_VREF_ICH IN 15
CK_66M_ICH IN 7 69

ICH_LAN_RXD0 IN 26 37
ICH_LAN_RXD1 IN 26 37
ICH_LAN_RXD2 IN 26 37
ICH_LAN_TXD0 OUT 26 37
ICH_LAN_TXD1 OUT 26 37
ICH_LAN_TXD2 OUT 26 37
R8E2 22 5% CH 603 0 1A SB
ICH_LAN_RST OUT 26 37
ICH_LAN_CLK IN 37
ICH_EE_DIN IN 26 37
ICH_EE_CS OUT 26 37
ICH_EE_CLK OUT 26 37
ICH_EE_DOUT OUT 25 26 37
AUD_LINK_SYNC_R OUT 25
AUD_LINK_SDO_R OUT 25 51
AUD_LINK_BCLK OUT 36 38
AUD_LINK_RST* OUT 36 38
AUD_LINK_SDI0_CNR IN 36
AUD_LINK_SDI1_CNR IN 36
AUD_LINK_SDI2 OUT 25 36 38

R7E8 22.6 1% 603 CH SB
USBRBIAS

CADNOTE:
LESS THAN 500 MILS
FROM ICH

#1 FOR DEBUG ONLY

LPC/HI/LAN/AC97/USB/GPIO/MISC

[PAGE_TITLE=ICH4_B]

DRAWING
FAB_A.SCH.1.24
Mon Nov 18 12:45:01 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	24	4.0

ATTRIBUTES:

VCC3

ICT TEST SITE

R7F4 10K 5% EMPTY 603
R7F11 10M 5% CH 603
R7F1 10K 5% EMPTY 603
R7F6 10K 5% EMPTY 603
R7F5 10K 5% CH 603
R7F8 10K 5% CH 603
R7F2 10K 5% CH 603
R7F7 10K 5% CH 603

DEBUG ONLY
R9G5 0 603 1A CH

23 IN ICH_P_PCIRST* → P_PCIRST* OUT 59 11 46 51 52 74 75 76

BOARDID<3..0> BI 24

C9G2 47PF 5% 50V NPO 603

TERMINATION FOR INTEGRATED AUDIO

NOTE:
R7X12 IS ALWAYS STUFFED.

24 IN AUD_LINK_SDO_R → R9D6 33 603 5% CH → AUD_LINK_SDO_CNR OUT 36
AUD_LINK_SDO_R → R9D5 33 603 5% CH → AUD_LINK_SDO_CDC OUT 38
24 IN AUD_LINK_SYNC_R → R9D3 33 603 5% CH → AUD_LINK_SYNC_CNR OUT 36
AUD_LINK_SYNC_R → R9D4 33 603 5% CH → AUD_LINK_SYNC_CDC OUT 38

69 63 IN V_3P3_STBY — C7E6 .1UF 20% 25V Y5V 603 — C8F3 .1UF 20% 25V Y5V 603
63 IN V_1P5_STBY — C8G2 .1UF 20% 25V Y5V 603 — C7E5 .1UF 20% 25V Y5V 603

66 IN V_1P5_CORE — C7F5 .1UF 20% 25V Y5V 603 — C7F7 .1UF 20% 25V Y5V 603 — C7F9 .1UF 20% 25V Y5V 603 — C7F4 .1UF 20% 25V Y5V 603

CAD NOTE:
PLACE WITHIN 40 MILS OF ICH

61 IN V_3P0_BAT_VREG — C8F1 .1UF 20% 25V Y5V 603 — C7G1 .1UF 20% 25V Y5V 603
52 IN V_REF5V — C8F2 .1UF 20% 25V Y5V 603 — C8G3 .1UF 20% 25V Y5V 603
69 67 IN VCCP — C8E6 .1UF 20% 25V Y5V 603 — C8E5 .1UF 20% 25V Y5V 603
52 IN V_REF5V_SUS — C7F10 .1UF 20% 25V Y5V 603 — C8E7 .1UF 20% 25V Y5V 603

66 IN V_1P5_CORE

VCC3

R7F13 68.1 1% CH 603
R9G4 10K 5% CH 603
R7F16 10K 5% CH 603
R9G1 4.7K 5% CH 603
R7F3 10K 5% CH 603
R7F10 62 5% CH 603

HI_RCOMP_ICH OUT 24
ICH_THRM_PU* OUT 24
ICH_VRMPWRGD_PU OUT 24
ICH_GPIO6_GPIO7 OUT 24
APICD0_1 OUT 24
HI<11> OUT 24

ICH_EE_DOUT OUT 24 26 37
R9D8 10K 5% EMPTY 603

2 R9D7 1 AUD_LINK_SDI2 OUT 24 36 38
8.2K 603 5% CH

1 R8G12 2 330K 603 5% CH
1 J9G3 1X2HDR HDR
INTRUDER* OUT 24
ICH_RTCRST OUT 24

61 IN V_3P0_BAT_VREG — R8G10 22K 603 5% CH — C8G9 10UF 10% 10V Y5V 805 603

J9J1 1X3HDR HDR
TP_CLRCMOS
NET_CLR_CMOS_JUMPER
R8J2 4.7K 5% CH 603

1-2	NORMAL
2-3	CLR CMOS

V_3P3_STBY IN 63 69

R9G7 10K 5% CH 603
R8G2 10K 5% CH 603
R8G1 8.2K 5% CH 603
R8G3 10K 5% CH 603
R8G4 10K 5% CH 603
R9G8 10K 5% EMPTY 603

SUS_STAT_PU* OUT 24
SMB_ALERT_PU OUT 24
ICH_RI_PU OUT 24
ICH_TP0_PU OUT 24
ICH_GPIO8 OUT 24

61 IN V_BAT_VREG_R_CR — C8G6 .047UF 20% 50V X7R 603 — C8G7 1UF 10% 16V Y5V EMPTY 603

R8G7 10M 603 5% CH
ICH_VBIAS OUT 24
ICH_RTCX1 OUT 24
ICH_RTCX2 OUT 24

A52705-003
Y8G1 SOCKET TH CONN

NOTE:
ADD XTAL PART # 107930-002 TO BOM BY USING MOD FILE

R8G9 10M 603 5% CH
C8G8 10PF 5% 50V NPO 603
C8G10 10PF 5% 50V NPO 603

ICH PULLUPS & DECOUPLING

DRAWING
FAB_A.SCH.1.25
Mon Nov 18 12:45:11 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	25	4.0

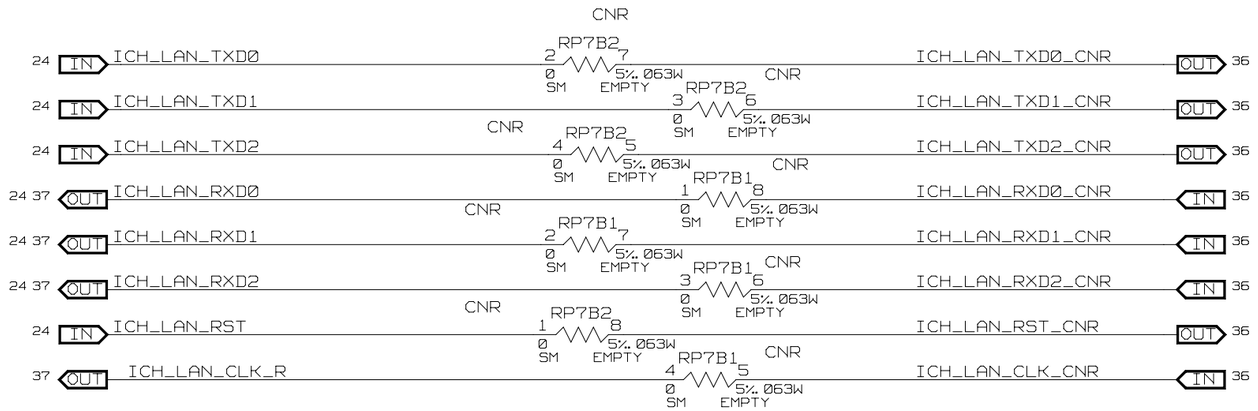
[PAGE_TITLE=ICH4_C]

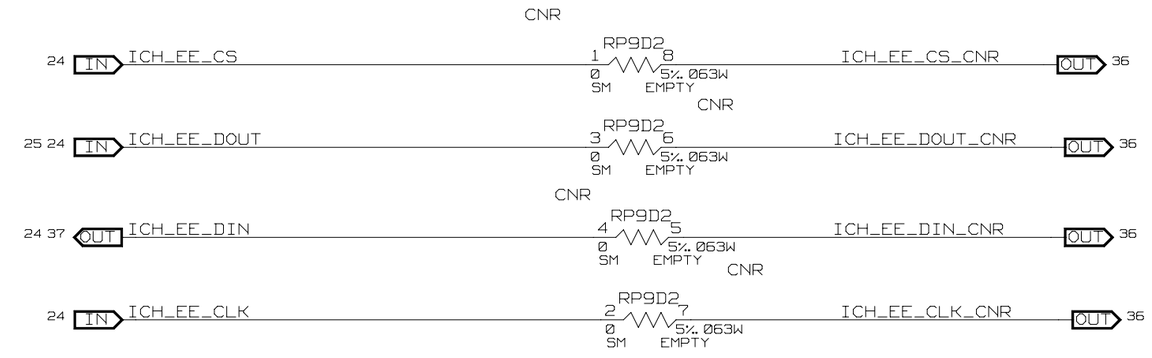
ICH AND CNR LINK STUFFING OPTION PAGE

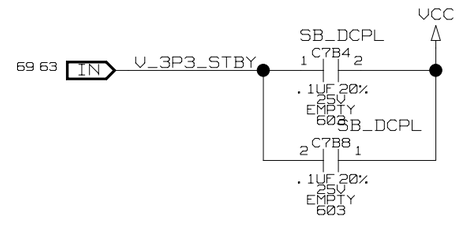
CAD NOTE:

PLACE THESE R-PACKS UNDERNEATH
THE LAN CHIP, RIGHT BY THE PINS TO
MINIMIZE STUB FROM PIN TO R-PACK

STUFF ONLY WHEN YOU HAVE CNR AND NO LAN.







0-OHMS ARE PROVIDED
TO MINIMIZE STUBS
ON LAN INTERFACE

[PAGE_TITLE=ICH_360]

DRAWING
FAB_A.SCH.1.26
Mon Nov 18 12:45:21 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	26	4.0

DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

VCC3
IDE
R8G5 2 1 4.7K 603 5% CH

IDE
R7G5 2 1 8.2K 603 5% CH

VCC3
IDE
R7G6 2 1 4.7K 603 5% CH

IDE
R7G7 2 1 8.2K 603 5% CH

52 IN IDE_RST*

23 OUT ICH_IDE_PDDREQ
23 IN ICH_IDE_PDIOW*
23 IN ICH_IDE_PDIOR*
23 OUT ICH_IDE_PIORDY
23 IN ICH_IDE_PDDACK*
23 OUT ICH_IDE_IRQ14
23 IN ICH_IDE_PDA<1>
23 IN ICH_IDE_PDA<0>
23 IN ICH_IDE_PDCS1*
23 IN ICH_IDE_PDCS3*
23 IN ICH_IDE_PDA<2>

23 OUT ICH_IDE_SDDREQ
23 IN ICH_IDE_SDIOW*
23 IN ICH_IDE_SDIOR*
23 OUT ICH_IDE_SIORDY
23 IN ICH_IDE_SDDACK*
23 OUT ICH_IDE_IRQ15
23 IN ICH_IDE_SDA<1>
23 IN ICH_IDE_SDA<0>
23 IN ICH_IDE_SDCS1*
23 IN ICH_IDE_SDCS3*
23 IN ICH_IDE_SDA<2>

23 IN ICH_IDE_SDD<15..0>
23 IN ICH_IDE_PDD<15..0>

IDE
R6H3 2 1 33 603 5% CH

IDE
R6H2 2 1 33 603 5% CH

IDE
J6H2
2X20HDR_20
IDE_PRI_RST_R
TP_IDE_PRI_32
HDR

IDE
J6H1
2X20HDR_20
IDE_SEC_RST_R
TP_IDE_SEC_32
HDR

PRIMARY IDE CONNECTOR

SECONDARY IDE CONNECTOR

GPIO_DMA66_DETECT_PRI OUT 51
IDE_PRI_ACT* OUT 52

GPIO_DMA66_DETECT_SEC OUT 51
IDE_SEC_ACT* OUT 52

IDE
C9H5 1 2 .047UF 20% 50V EMPTY 603 "X7R" (+/- 10%)
R9H11 2 1 15K 603 5% CH

IDE
C9H3 1 2 .047UF 20% 50V EMPTY 603 "X7R" (+/- 10%)
R9H9 2 1 15K 603 5% CH

CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

ROOM = IDE EXCEPT WHERE NOTED

[PAGE_TITLE=IDE_SOUTH_BRIDGE]

DRAWING
FAB_A.SCH.1.27
Mon Nov 18 12:45:32 2002
D845GET FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	27	4.0

PCI IDE

COMPONENTS ARE DFM29

62 IN VREG_USB_BP_LEFT

29 24 BI USB_BPL_P2*

29 24 BI USB_BPL_P2

L6B2
90OHM
IND 4PIN

29 USB_BACK1_R*

29 USB_BACK1_R

USB
CR6A1
EMPTY
PGB0010603

USB
CR6A2
EMPTY
PGB0010603

29 24 BI USB_BPL_P0*

29 24 BI USB_BPL_P0

L6B1
90OHM
IND 4PIN

29 USB_BACK2_R*

29 USB_BACK2_R

USB
CR6A3
EMPTY
PGB0010603

USB
CR6A4
EMPTY
PGB0010603

USB
C5A1
470PF
10%
50V
X7R
603

LEFT
USB_BPL
A14537-002
NORES
JA5A1
2 X USB
IO

NOTE:
USE 749193-001 FOR
2X USB WHEN NOT USING
MAGJACK OR THE SINGLE STACK

62 IN VREG_USB_BP_RIGHT

29 BI USB_BPR_P1*

29 BI USB_BPR_P1

L2A2
90OHM
IND 4PIN

29 USB_BACK3_R*

29 USB_BACK3_R

EMPTY

USB
CR2A3
EMPTY
PGB0010603

USB
CR2A4
EMPTY
PGB0010603

29 24 BI USB_BPR_P4*

29 24 BI USB_BPR_P4

L2A1
90OHM
IND 4PIN

29 USB_BACK4_R*

29 USB_BACK4_R

USB
CR2A1
EMPTY
PGB0010603

USB
CR2A2
EMPTY
PGB0010603

USB
C2A1
470PF
10%
50V
X7R
603

RIGHT
USB_BPR
749193-001
J2A2
2 X USB
CONN

NOTE
WHEN NOT ROUTING USB PORT 2
TO CNR STUFF SINGLE STACK
CONNECTOR. IPN 749193-002
STUFF ON PORT 3 PAIR

CAD NOTE:
PLACE NEAR USB CONN

DRAWING
FAB_A.SCH.1.28
Mon Nov 18 13:49:35 2002
D845GFT FAB_A

[PAGE_TITLE=BACKPANEL_USB_LEFT]

	DOCUMENT NUMBER	PAGE	REV
	C23021	28	4.0

NOTE:
STUFF THESE 3 RESISTORS WHEN SUPPORTING 4 USB PORTS
OUT THE BACKPANEL AND NO CNR CONNECTOR.

DEBUG
1 R9B172 0 402 5% EMPTY
USB_BPR_P1* BI 28 29

FOR DEBUG ONLY
24 BI USB_ICH_P1*
1 R9B142 0 402 5% CH
USB_CNR_P1* BI 36

DEBUG
24 BI USB_ICH_P1
1 R9B132 0 402 5% CH
USB_CNR_P1 BI 36
DEBUG

DEBUG
1 R9B162 0 402 5% EMPTY
USB_BPR_P1 BI 28 29

DEBUG
62 IN USB_ICH_BPR_OC*
1 R7E6 2 0 603 1A EMPTY
USB_ICH_CNR_OC* OUT 30 24

DEBUG
29 28 24 IN USB_BPL_P0
1 R7T1 2 0 603 1A EMPTY
USB_BPL_P0 OUT 24 28 29

DEBUG
29 28 24 IN USB_BPL_P0*
1 R7T2 2 0 603 1A EMPTY
USB_BPL_P0* OUT 24 28 29

DEBUG
28 24 IN USB_BPL_P2
1 R6B3 2 0 603 1A EMPTY
USB_BACK1_R OUT 28

DEBUG
28 24 IN USB_BPL_P2*
1 R6B4 2 0 603 1A EMPTY
USB_BACK1_R* OUT 28

DEBUG
29 28 24 IN USB_BPL_P0
1 R6B1 2 0 603 1A EMPTY
USB_BACK2_R OUT 28

DEBUG
29 28 24 IN USB_BPL_P0*
1 R6B2 2 0 603 1A EMPTY
USB_BACK2_R* OUT 28

NOTE:
FOR DEBUG ONLY

DEBUG
29 28 IN USB_BPR_P1
1 R2A4 2 0 603 1A EMPTY
USB_BACK3_R OUT 28

DEBUG
29 28 IN USB_BPR_P1*
1 R2A3 2 0 603 1A EMPTY
USB_BACK3_R* OUT 28

DEBUG
28 24 IN USB_BPR_P4
1 R2A2 2 0 603 1A EMPTY
USB_BACK4_R OUT 28

DEBUG
28 24 IN USB_BPR_P4*
1 R2A1 2 0 603 1A EMPTY
USB_BACK4_R* OUT 28

[PAGE_TITLE=BLANK]

DRAWING
FAB_A.SCH.1.29
Mon Nov 18 13:49:44 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	29	4.0

CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING

CAD NOTE: PLACE MIDWAY BETWEEN THE FPANEL (2X5) & CNR
RUN MUST HAVE 50 MIL POWER TO BOTH LOCATIONS.

VCC
U7H1
SI4501DY
61 IN VREG_USB_NCH 2 G1 DRN 7
69 60 IN V_5P0_STBY 3 S2 DRN 6
61 IN VREG_USB_PCH 4 G2 DRN 5
1 S1 DRN 8
IC A03106-001
NOTE: .1 INCH COPPER ON DRAIN AND SOURCE

R8H17 150K 5% CH 603

STUFF FOR NON-FUSED FRONT PANEL SUPPORT

RT7H1 THRMSTR 1.50
R7H11 0 805 1A EMPTY
R7H10 0 805 1A EMPTY

USB_CNR_PWR OUT 30 36
USB_FP_PWR OUT 30

1C7H2 220UF 20% 25V TLEC RDL 201307-001

NOTE:
RPD ASSUMES FPANEL CARD
HAS THERM & PROVIDES OC#

CAD NOTE:
LEAVE ROOM FOR 2 CHOKES,
1 THERMISTER AND 1 TH CAP.

69 63 IN V_3P3_STBY

R7H7 10K 5% EMPTY 603
R8H11 10K 5% EMPTY 603

USB_ICH_FP_OC* OUT 24
USB_ICH_CNR_OC* OUT 29 24

Q7H1 MBT3904DUAL

69 52 IN PWRGD_3V
R7H6 1K 5% EMPTY 603
R7H8 1K 5% EMPTY 603
EMPTY

30 IN USB_FP_OC_R*
36 IN USB_CNR_OC*
R7H3 0 603 1A CH
R7H1 0 603 1A CH

R7H4 10K 5% CH 603
R7H2 10K 5% CH 603

30 IN USB_CNR_PWR

USB_FP
J7H1
2X5HDR_9
HDR

24 BI USB_FP_P5*
24 BI USB_FP_P5
USB_FP_P3*
USB_FP_P3
BI 24
BI 24

NET_USB_FNT_P10

USB_FP
C7H4 470PF 10% 50V CER EMPTY 603
C7H3 470PF 10% 50V CER EMPTY 603

USB_FP
R7H9 0 805 1A EMPTY
STUFF FOR NON-FUSED FRONT PANEL SUPPORT

STUFF FOR FUSED FRONT PANEL SUPPORT
R7H5 0 1A EMPTY 603 USB_FP

USB_FP
R7H12 0 805 1A CH
30 IN USB_FP_PWR
USB_FP_OC_R* OUT 30

STUFF FOR FUSED FRONT PANEL SUPPORT

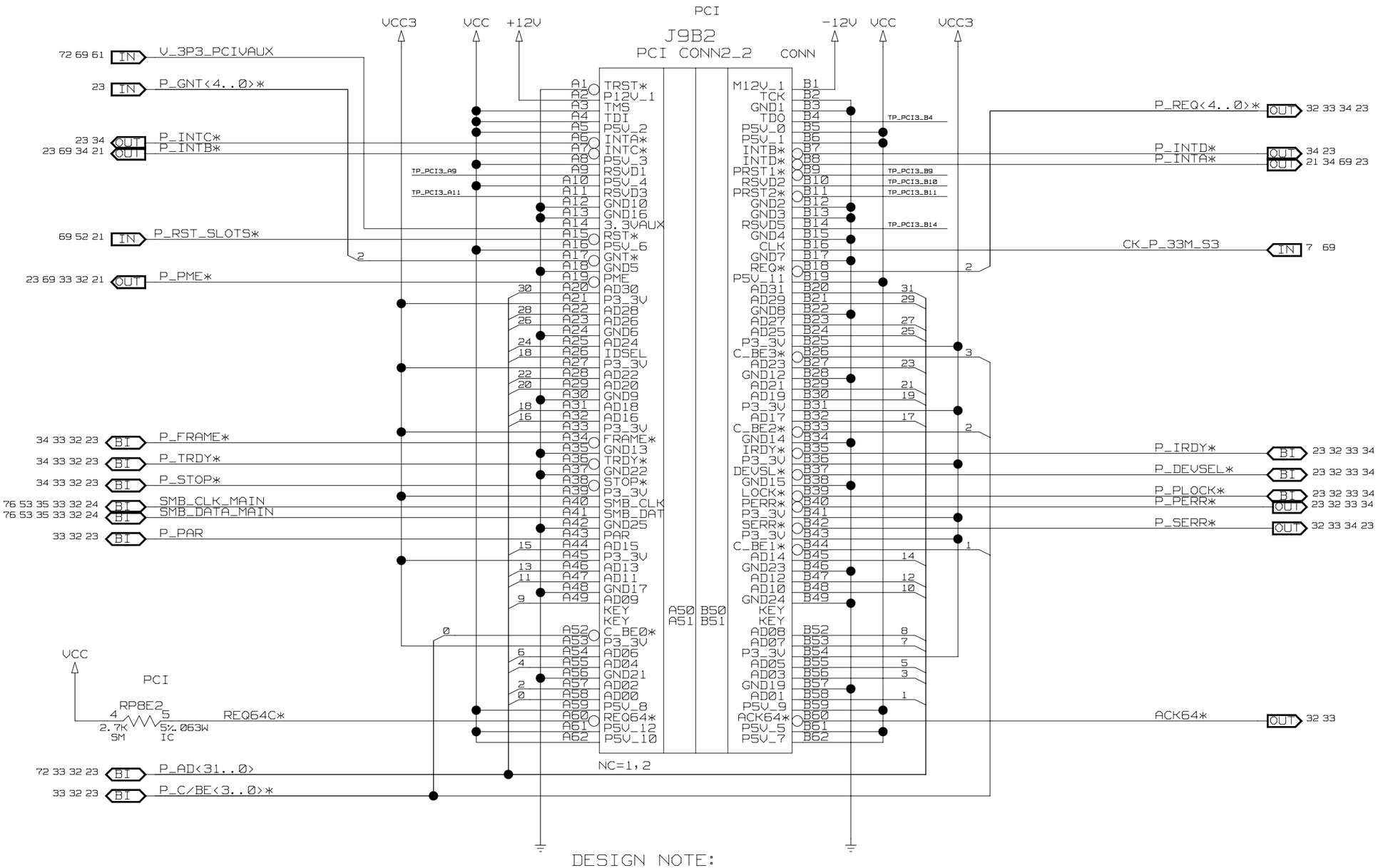
USB FNT PANEL POWER

[PAGE_TITLE=USB_FP_HEADER_POWER]

DRAWING
FAB_A.SCH.1.30
Mon Nov 18 13:49:53 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	30	4.0

PCI SLOT 3



DESIGN NOTE:

PCI SLOT3 = PCI DEVICE #18
REQ/GNT PAIR = #2
IRQ MAP A : B : C : D
C : D : B : A

PCI SLOT 3

[PAGE_TITLE=PCI_SLOT3]

DRAWING
FAB_A.SCH.1.31
Mon Nov 18 13:50:03 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	31	4.0

PCI SLOT 2

PCI
J8B2
PCI CONN2_2 CONN

	A		B
	TRST*	M12V_1	
	P12V_1	TCK	
	TMS	GND1	
	TDI	TDO	TP_PCI2_B4
	P5V_2	P5V_0	
	INTA*	P5V_1	
	INTC*	INTB*	
	P5V_3	INTD*	
TP_PCI2_A9	RSVD1	PRST1*	TP_PCI2_B9
	P5V_4	RSVD2	
	RSVD3	PRST2*	TP_PCI2_B11
	GND10	GND2	
	GND16	GND3	
	3.3VAUX	RSVD5	
	RST*	GND4	
	P5V_6	CLK	
1	GNT*	GND7	
	GND5	REQ*	1
PCI_SLOT_2_PME_A19	PME	P5V_11	
30	AD30	AD31	31
	P3_3V	AD29	29
28	AD28	GND8	
26	AD26	AD27	27
	GND6	AD25	25
24	AD24	P3_3V	
	IDSEL	C_BE3*	3
	P3_3V	AD23	23
22	AD22	GND12	
20	AD20	AD21	21
	GND9	AD19	19
18	AD18	P3_3V	
16	AD16	AD17	17
17	P3_3V	C_BE2*	2
	FRAME*	GND14	
	GND13	IRDY*	
	TRDY*	P3_3V	
	GND22	DEVSL*	
	STOP*	GND15	
	P3_3V	LOCK*	
	SMB_CLK	PERR*	
	SMB_DAT	P3_3V	
	GND25	SERR*	
	PAR	P3_3V	
15	AD15	C_BE1*	1
	P3_3V	AD14	14
13	AD13	GND23	
11	AD11	AD12	12
	GND17	AD10	10
9	AD09	GND24	
	KEY	KEY	
	KEY	KEY	
0	C_BE0*	AD08	8
	P3_3V	AD07	7
6	AD06	P3_3V	
4	AD04	AD05	5
	GND21	AD03	3
2	AD02	GND19	
0	AD00	AD01	1
	P5V_8	P5V_9	
	REQ64*	ACK64*	
	P5V_12	P5V_5	
	P5V_10	P5V_7	

A50 B50
A51 B51

NC=1,2

72 OUT DEBUG_PCI2_A14_AUX

CUSTOM_MOON_ISA

72 69 61 IN V_3P3_PCIVAUX — 1 R8C1 2 — 0 603 — 1A EMPTY

23 IN P_GNT<4..0>*

23 34 33 OUT P_INTG*
23 34 33 OUT P_INTE*

72 IN DEBUG_PCI2_A11_RSVD3

69 52 21 IN P_RST_SLOTS*

CUSTOM_MOON_ISA

23 69 33 31 21 OUT P_PME* — 1 R8C2 2 — 0 603 — 1A CH

CUSTOM_MOON_ISA

72 OUT PCI_SLOT2_IDSEL

1 R8C3 2 — 0 603 — 1A EMPTY

CUSTOM_MOON_ISA

1 R8C4 2 — 0 603 — 1A EMPTY

34 33 31 23 BI P_FRAME*
34 33 31 23 BI P_TRDY*
34 33 31 23 BI P_STOP*

76 53 35 33 31 24 BI SMB_CLK_MAIN
76 53 35 33 31 24 BI SMB_DATA_MAIN

33 31 23 BI P_PAR

VCC

PCI

RP8E2 — 3 — 6 — 2.7K SM — 5% .063W IC

REQ64B*

72 33 31 23 BI P_AD<31..0>

33 31 23 BI P_C/BE<3..0>*

P_REQ<4..0>* OUT 31 33 34 23

P_INTF* OUT 33 34 23
P_INTH* OUT 33 34 23

DEBUG_PCI2_B10_RSVD2 OUT 72

DEBUG_PCI2_B14_RSVD5 IN 72

CK_P_33M_S2 IN 7 69

P_IRDY* BI 23 31 33 34

P_DEVSEL* BI 23 31 33 34

P_PLOCK* BI 23 31 33 34
P_PERR* OUT 23 31 33 34

P_SERR* OUT 31 33 34 23

ACK64* OUT 31 33

DESIGN NOTE:

PCI SLOT2 = PCI DEVICE #17/22
REQ/GNT PAIR = #1
IRQ MAP A : B : C : D
G : F : E : H

[PAGE_TITLE=PCI_SLOT2]

DRAWING
FAB_A.SCH.1.32
Mon Nov 18 13:50:14 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	32	4.0

PCI SLOT 1
CLOSEST TO AGP

PCI J7B1
PCI CONN2_2 CONN

VCC3 VCC +12V -12V VCC VCC3

72 69 61 IN V_3P3_PCIVAUX
23 IN P_GNT<4..0>*
23 34 32 OUT P_INTF*
23 34 32 OUT P_INTH*
69 52 21 IN P_RST_SLOTS*
23 69 32 31 21 OUT P_PME*
34 32 31 23 BI P_FRAME*
34 32 31 23 BI P_TRDY*
34 32 31 23 BI P_STOP*
76 53 35 32 31 24 BI SMB_CLK_MAIN
76 53 35 32 31 24 BI SMB_DATA_MAIN
32 31 23 BI P_PAR
72 32 31 23 BI P_AD<31..0>
32 31 23 BI P_C/BE<3..0>*

P_REQ<4..0>* OUT 31 32 34 23
P_INTG* OUT 32 34 23
P_INTE* OUT 32 34 23
CK_P_33M_S1 IN 7 69
P_IRDY* BI 23 31 32 34
P_DEVSEL* BI 23 31 32 34
P_PLOCK* BI 23 31 32 34
P_PERR* OUT 23 31 32 34
P_SERR* OUT 31 32 34 23
32 31 IN ACK64*

	TP_PCI1_A1	A1	TRST*	M12V_1	B1		
		A2	P12V_1	TCK	B2		
	TP_PCI1_A3	A3	TMS	GND1	B3		
	TP_PCI1_A4	A4	TDI	TDO	B4		TP_PCI1_B4
		A5	P5V_2	P5V_0	B5		
		A6	INTA*	P5V_1	B6		
		A7	INTC*	INTB*	B7		
		A8	P5V_3	INTD*	B8		
	TP_PCI1_A9	A9	RSVD1	PRST1*	B9		TP_PCI1_B9
		A10	P5V_4	RSVD2	B10		TP_PCI1_B10
	TP_PCI1_A11	A11	RSVD3	PRST2*	B11		TP_PCI1_B11
		A12	GND10	GND2	B12		
		A13	GND16	GND3	B13		
		A14	3.3VAUX	RSVD5	B14		TP_PCI1_B14
		A15	RST*	GND4	B15		
		A16	P5V_6	CLK	B16		
		A17	GNT*	GND7	B17		
		A18	GND5	REQ*	B18	0	
		A19	PME	P5V_11	B19		
	30	A20	AD30	AD31	B20	31	
		A21	P3_3V	AD29	B21	29	
	28	A22	AD28	GND8	B22		
	26	A23	AD26	AD27	B23	27	
		A24	GND6	AD25	B24	25	
	24	A25	AD24	P3_3V	B25		
	16	A26	IDSEL	C_BE3*	B26	3	
		A27	P3_3V	AD23	B27	23	
	22	A28	AD22	GND12	B28		
	20	A29	AD20	AD21	B29	21	
		A30	GND9	AD19	B30	19	
	18	A31	AD18	P3_3V	B31		
	16	A32	AD16	AD17	B32	17	
		A33	P3_3V	C_BE2*	B33	2	
		A34	FRAME*	GND14	B34		
		A35	GND13	IRDY*	B35		
		A36	TRDY*	P3_3V	B36		
		A37	GND22	DEVSL*	B37		
		A38	STOP*	GND15	B38		
		A39	P3_3V	LOCK*	B39		
		A40	SMB_CLK	PERR*	B40		
		A41	SMB_DAT	P3_3V	B41		
		A42	GND25	SERR*	B42		
		A43	PAR	P3_3V	B43		
	15	A44	AD15	C_BE1*	B44	1	
		A45	P3_3V	AD14	B45	14	
	13	A46	AD13	GND23	B46		
	11	A47	AD11	AD12	B47	12	
		A48	GND17	AD10	B48	10	
	9	A49	AD09	GND24	B49		
			KEY	KEY			
			KEY	KEY			
		A52	C_BE0*	AD08	B52	8	
		A53	P3_3V	AD07	B53	7	
	6	A54	AD06	P3_3V	B54		
	4	A55	AD04	AD05	B55	5	
		A56	GND21	AD03	B56	3	
	2	A57	AD02	GND19	B57		
	0	A58	AD00	AD01	B58	1	
		A59	P5V_8	P5V_9	B59		
		A60	REQ64*	ACK64*	B60		
		A61	P5V_12	P5V_5	B61		
		A62	P5V_10	P5V_7	B62		

A50 B50
A51 B51

NC=1,2

VCC
PCI
RP8E2
1 8 REQ64A*
2.7K 5% .063W
SM IC

VCC
PCI
RP8E2
7 2
2.7K 5% .063W
SM IC

DESIGN NOTE:

PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
F : G : H : E

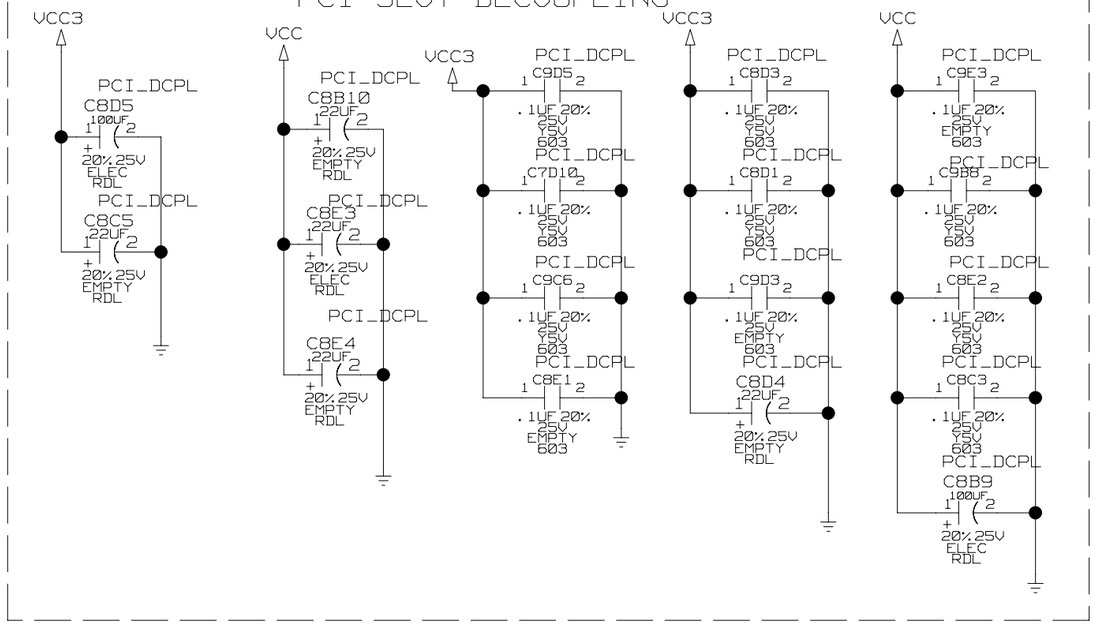
DRAWING
FAB_A.SCH.1.33
Mon Nov 18 13:50:24 2002
D845GFT FAB_A

PCI SLOT 1

[PAGE_TITLE=PCI_SLOT1]

DOCUMENT NUMBER	PAGE	REV
C23021	33	4.0

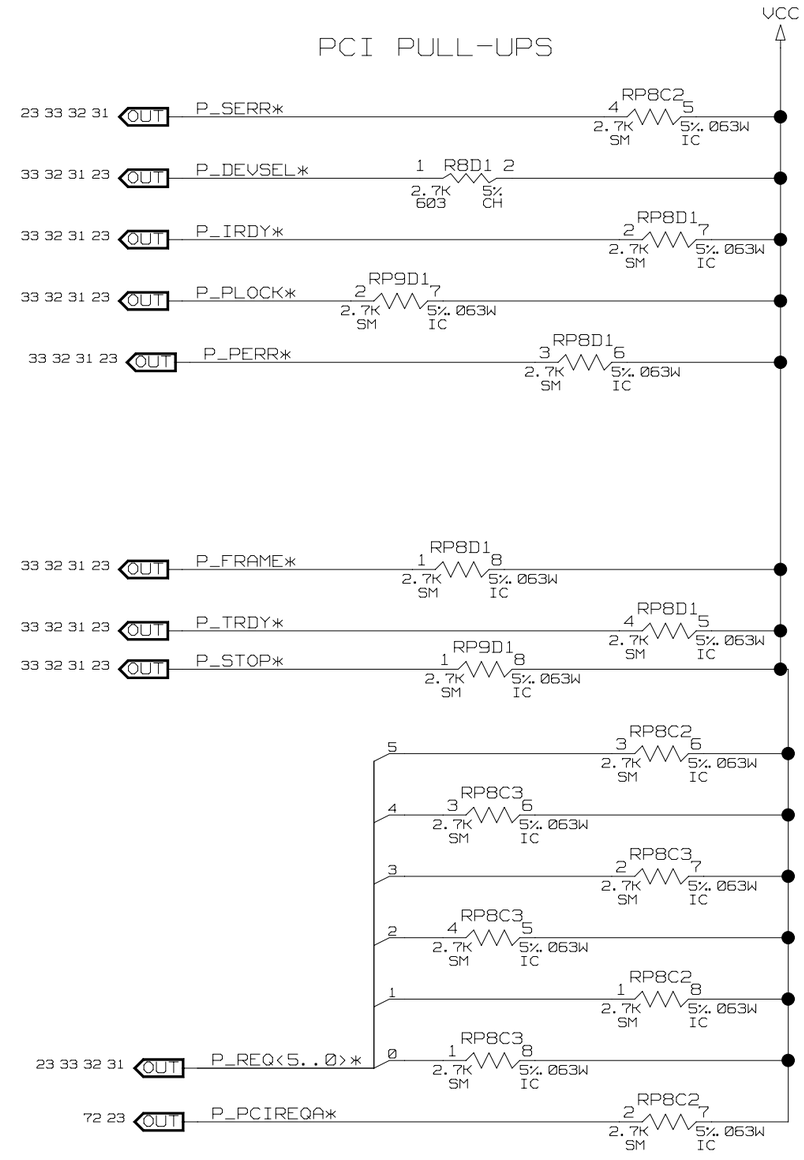
PCI SLOT DECOUPLING

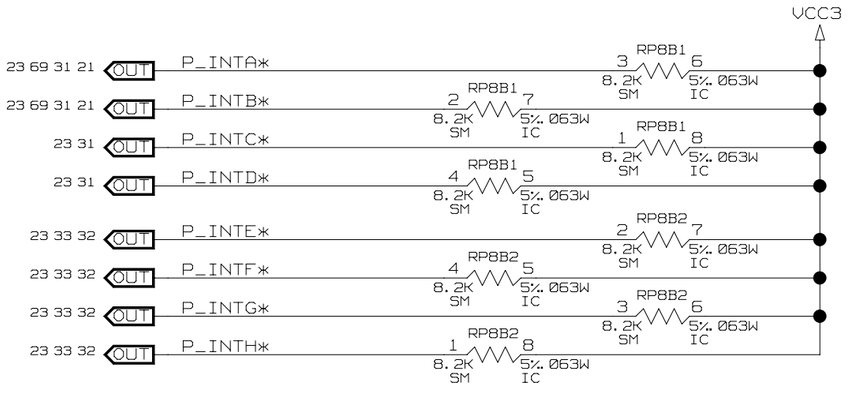


NOTE

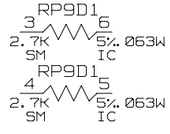
PLOCK, PSTOP, PTRDY, PIRDY, PFRAME, PPERR MAY NEED TO BE CHANGED TO A 3.3V PU

PCI PULL-UPS





SPARE SECTIONS



[MODULE=ICH]

[PAGE_TITLE=ICH_PCI_TERMINATION]

DRAWING
FAB_A.SCH.1.34
Mon Nov 18 12:46:34 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	34	4.0

69 63 IN V_3P3_STBY

SB R9G11 1.5K 5% CH 603

SB R9G14 1.5K 5% CH 603

76 53 33 32 31 24 BI SMB_CLK_MAIN

76 53 33 32 31 24 BI SMB_DATA_MAIN

VCC

SB R9G10 2.7K 5% CH 603

SB Q9G3 FET

SB R8J1 0 1A EMPTY 603

SB Q9G2 FET

SB R8J3 0 1A EMPTY 603

52 IN PWRGD_PS_BUFF

SB R9G9 10K 603 5% CH

PWRGD_PS_BUFF_OC_R

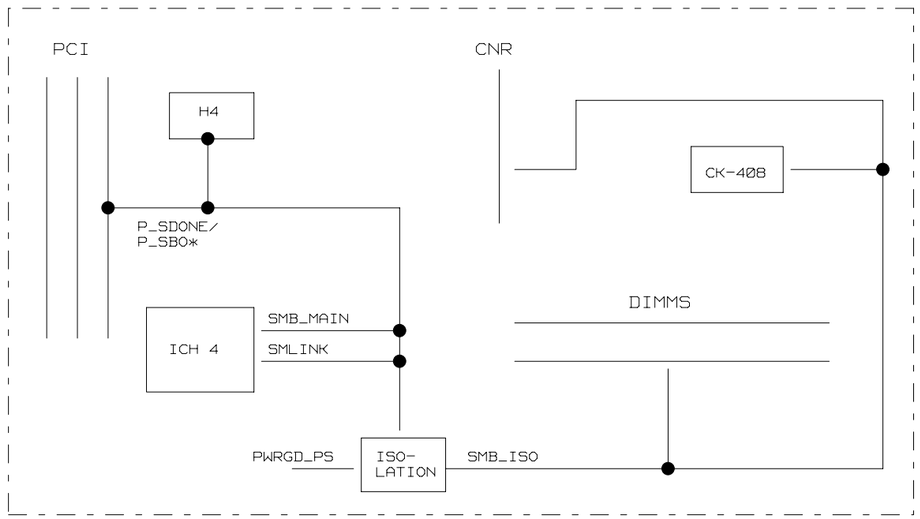
VCC3

SB R9G13 8.2K 5% CH 603

SB R9G12 8.2K 5% CH 603

69 36 17 7 BI SMB_CLK_ISO

69 36 17 7 BI SMB_DATA_ISO



[PAGE_TITLE=SMBUS_ISOLATION]

DRAWING FAB_A.SCH.1.35
Mon Nov 18 12:46:44 2002
D845GFI FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	35	4.0

[DONOR_REV=1.02/page59] [DONOR_PROJ=NBVV_DDR--1130]
[PROJ_REV=2.00/page25] [PROJ_NAME= _G_DDR--1164]
[MODULE=ICH]
[SOLUTION=INTEL/ICH1_82801]
[MOD_PAGE=page24]
[LAST_MAKEPROJ: 10/12/2001 1:56:55 PM]
[MOD_REV=1.0.35]

NOTE: CNR SPEC SAYS SMBUS CONTROLLER NOT POWERED BY 3V STBY

SMB ADDRESS: 1101110
WRITE DC
READ DD

CNR SLOT DECOUPLING
VCC
C9C4 10.0UF 20% 6.3V EMPTY 1206
VCC3
C9C5 .1UF 20% 25V EMPTY 603
+12V
C9C1 .1UF 20% 25V EMPTY 603

J9B1
CNR60

TP_CNR_B1	B1	RESERVED	RESERVED	A1	TP_CNR_A1
TP_CNR_B2	B2	RESERVED	RESERVED	A2	TP_CNR_A2
TP_CNR_B3	B3	RESERVED	GND	A3	
	B4	GND	RESERVED	A4	TP_CNR_A4
TP_CNR_B5	B5	RESERVED	RESERVED	A5	TP_CNR_A5
TP_CNR_B6	B6	RESERVED	GND	A6	
	B7	GND	LAN_TXD2	A7	ICH_LAN_TXD2_CNR IN 26
26 IN	B8	LAN_TXD1	LAN_TXD0	A8	ICH_LAN_TXD0_CNR IN 26
26 IN	B9	LAN_RSTSYNC	GND	A9	
	B10	GND	LAN_CLK	A10	ICH_LAN_CLK_CNR OUT 26
26 OUT	B11	LAN_RXD2	LAN_RXD1	A11	ICH_LAN_RXD1_CNR OUT 26
26 OUT	B12	LAN_RXD0	RESERVED	A12	TP_CNR_A12
	B13	GND	USB+	A13	USB_CNR_P1 BI 29
TP_CNR_B14	B14	RESERVED	GND	A14	
30 IN	B15	+5VDUAL	USB-	A15	USB_CNR_P1* BI 29
30 OUT	B16	USB_OC	+12V	A16	+12V
	B17	GND	GND	A17	
-12V	B18	-12V	+3.3VDUAL	A18	V_3P3_PCIVAUX IN 61 69 72
VCC3	B19	+3.3VD	+5VD	A19	VCC
	B20	GND	GND	A20	
26 OUT	B21	EEDO	EEDI	A21	ICH_EE_DOUT_CNR IN 26
26 IN	B22	EECK	EECS	A22	ICH_EE_CS_CNR IN 26
	B23	GND	SMB_A1	A23	
	B24	SMB_A0	SMB_A2	A24	
69 35 17 7 BI	B25	SMB_SCL	SMB_SDA	A25	SMB_DATA_ISO BI 7 17 35 69
36 24 OUT	B26	CDC_DWN_ENAB	AC97_RESET	A26	AUD_LINK_RST* IN 24
	B27	GND	AC97_SDATA_IN2	A27	
25 IN	B28	AC97_SYNC	AC97_SDATA_IN1	A28	CNR_SDI1_A28
25 IN	B29	AC97_SDATA_OUT	AC97_SDATA_IN0	A29	CNR_SDI0_A29
24 38 BI	B30	AC97_BITCLK	GND	A30	

CONN

AUD_LINK_SDI2_CNR
R9C6 2 0 603 1A CH
AUD_LINK_SDI1_CNR OUT 24
R9C7 2 0 603 1A CH
AUD_LINK_SDI0_CNR OUT 24
R9D2 2 0 603 1A CH DEBUG ONLY
J9D1 1X3HDR
AUD_LINK_SDI2 OUT 24 25 38

VCC3
STUFF FOR NO AUDIO DOWN
R7E7 100K 5% EMPTY 603

DYNAMIC PRIMARY DOWN CONTROL
STUFF FOR SOFT AUDIO W/CNR

69 63 IN V_3P3_STBY
PLACE BY PIN 14
C9F3 1UF 10% 25V X5R 603

24 IN AUD_LINK_RST*
24 IN GPO_AUD_EN*
36 24 BI CDC_DWN_ENAB*

DEBUG ONLY
R9F3 2 0 603 1A CH

R9F4 2 0 603 1A CH

U9F1 74LVC00A
VCC3=V_3P3_STBY(~PRIDWNCNTRL)
VCC3=14 GND=7

CDC_DWN_RST* OUT 38

AUD_LINK_RST*
IS DRIVEN BY
ICH4 ON
RESUME
WELL

R9F5 10K 5% CH 603

NEXT FAB SHOULD HAVE
A 0 OHM RESISTOR BETWEEN
PIN 1 AND PIN 2 OF U9F1.

PIN 1 WOULD GO TO R9F3.
PIN 2 WOULD GO TO R9F4.
WITH A RESITOR BETWEEN THEM.

STUFF FOR
CNR AND AUDIO

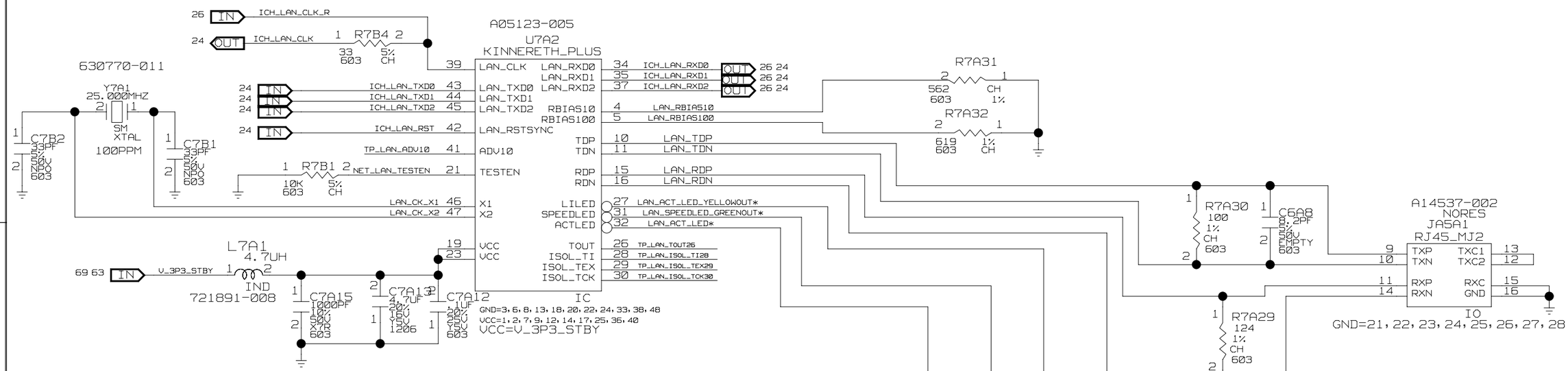
VCC
R9D1 10K 5% EMPTY 603
R9C1 10K 5% CH 603
R9C3 10K 5% CH 603
CNR_SMB_A0
CNR_SMB_A1
CNR_SMB_A2
R9C5 10K 5% CH 603
R9C2 10K 5% EMPTY 603
R9C4 10K 5% EMPTY 603

[MODULE=AUDIO]

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO]
[PAGE_TITLE=COMMUNICATION_NETWORK_RISER_&_DYNAMIC_PRIMARY_DOWN_CONTROL]
[MOD_PAGE=PAGE29] [MOD_REV=REV0_60C] [LAST_MAKEGOLD: 6/14/99 9:21:09am]

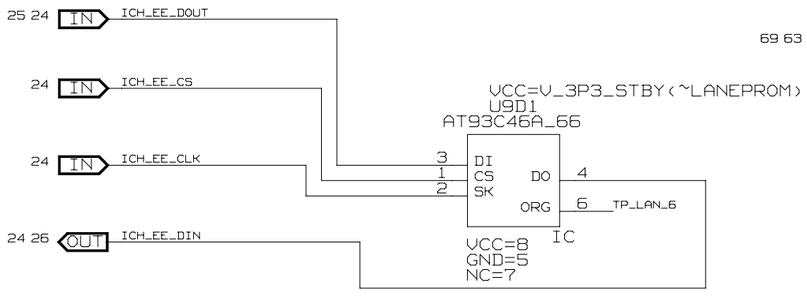
DRAWING FAB_A.SCH.1.36
Mon Nov 18 12:46:52 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	36	4.0

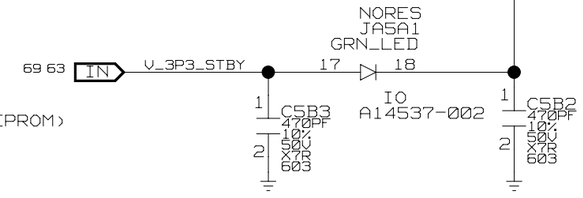


LAN E2 PROM

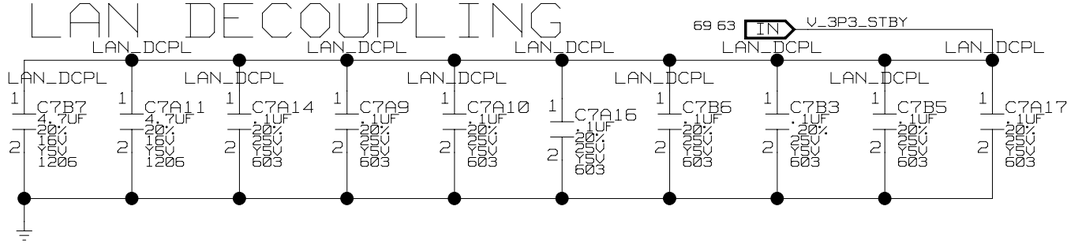
NOTE :
THE PART NUMBER REFLECTED IN THE CONCEPT LIBRARY IS A BLANK COMPONENT
PLEASE REFER TO LAN MANAGEABILITY WEB PAGE FOR INFORMATION REGARDING
THE CORRECT PART NUMBER FOR YOUR BOARDS FEATURE SET
HTTP://WWW-OPSD.INTEL.COM/LMM/LAN/DOCS/EEPROMBKM.DOC



BLANK PART # 109868-001
ATE PROGRAMMED PART # A70799-001
PRE-PROGRAMMED PART # A70876-001



LAN DECOUPLING



[PAGE_TITLE=LAN]

DRAWING
FAB_A.SCH.1.37
Mon Nov 18 12:47:02 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	37	4.0

25 IN AUD_LINK_SDO_CDC

25 IN AUD_LINK_SYNC_CDC

24 IN AUD_LINK_RST*

36 IN CDC_DWN_RST*

STUFF ONLY IF AUDIO PRESENT AND NO CNR

R9B5 0 5% 402 EMPTY

R9B6 1K 1% 402 CH

STUFF FOR CS4201 SUPPORT WITHOUT 24.576 XTAL

STUFF:
4201/05 = 0 OHM
9766 = EMPTY
1885/86 = EMPTY
1981 = 0 OHM

AUD_CK_24M_XTL_I

R9B2 0 5% 402 EMPTY

PLACE CAREFULLY / NO STUBS

AUD_XTAL

Y9A1 24.576MHZ SM XTAL 100 PPM

DEBUG R9A24 0 5% 402 CH

DEBUG R9B15 0 5% 402 CH

R9A23 0 5% EMPTY 402

C9A33 22PF 10% 50V NP0 402

AUD_XTAL

C9B2 22PF 10% 50V NP0 402

STUFF:
4205_PLL = 220PF
4201 = EMPTY
4205 = 220PF
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

FOR PLL MODE ONLY

AUD_CK_24M_XTL_O

R9B8 2.2K 5% EMPTY 402

STUFF:
4201/05 = 2.2K
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

R9B4 0 5% EMPTY 402

C9B4 .022UF 10% 50V X7R EMPTY 603

STUFF:
4201/05 = .022UF
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

STUFF:
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 0 OHM
1981 = EMPTY

R9B3 0 5% 402 EMPTY

CK_14M_AUD IN 7 69

R9A212 33 5% 402 CH

AUD_LINK_BCLK OUT 36 24

C9B5 5PF 5% 50V CH EMPTY 402

C9B1 10PF 5% 50V CH EMPTY 402

FOR PLL MODE ONLY

R9A16 1K 5% 402 EMPTY

STUFF:
4201/05 = EMPTY
9766 = 1K
1885/86 = EMPTY
1981 = 1K

R9A15 1K 5% 402 EMPTY

STUFF:
4201/05 = 0 OHM
9766 = EMPTY
1885/86 = EMPTY
1981 = 1K

24 IN SPKR

R9A222 10K 5% 402 CH

AUD_PCBEEP_IN_STAC9708_SPKR

R9A191 100 5% CH 402

C9A35 1UF 20% 16V Y5V 402

U9A1 AD1981

		2	XTL_IN		
		5	SDATA_OUT	XTL_OUT	3
		10	SYNC	BIT_CLK	6 AUD_LINK_BCLK_R
	CDC_RESET*	11	RESET	SDATA_IN	8 AUD_LINK_SDI2_R
	AUD_CODEC_ID0	45	ID0		
	AUD_CODEC_ID1	46	ID1		
44 IN	AUD_JS0	47	EAPD		
				SPDIF	48 AUD_SPDIF OUT 44 42
	AUD_PCBEEP_IN_STAC9708	12	NC_12	HP_OUT_L	39
		13	NC_13	HP_OUT_R	41
40 IN	AUD_PHONE				
40 IN	AUD_LAUXIN	14	NC_14		
40 IN	AUD_RAUXIN	15	NC_15		
44 IN	AUD_CODEC_I6	16	JS1		
44 IN	AUD_CODEC_I7	17	JS0	LINE_OUT_L	35 AUD_LINE_LOUT OUT 42
40 IN	AUD_LCD	18	CD_L	LINE_OUT_R	36 AUD_LINE_ROUT OUT 42
40 IN	AUD_CDGND	19	CD_GND	MONO_OUT	37 AUD_MONO_OUT OUT 40
40 IN	AUD_RCD	20	CD_R		
41 IN	AUD_MIC_IN	21	MIC1		
		22	NC_22		
40 IN	AUD_LLINEIN	23	LINE_IN_L		
40 IN	AUD_RLINEIN	24	LINE_IN_R		
39 OUT	AUD_3D_C	34	AVDD4	REFFLT	27
	AUD_DVDD1	1	DVDD1	VREFOUT	28
		9	DVDD2	AFLT1	29
		4	DVSS1	AFLT2	30
		7	DVSS2	AFLT3	31
		25	AVDD1	AFLT4	32
		38	AVDD2	AVSS4	33
		26	AVSS1	AVDD3	43
		42	NC	AVSS3	44
		NC=49		AVSS2	40 IC

R9A202 33 5% 402 CH

AUD_LINK_SDI2 OUT 24 25 36

V_5P0_AUD_ANALOG IN 45

R9A3 330K 5% EMPTY 402

R9A4 330K 5% EMPTY 402

STUFF:
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 330K
1981 = EMPTY

AUD_CDC_LOUT OUT 42

AUD_CDC_ROUT OUT 42

40 IN AUD_PHONE

43 IN

42 IN SPDIF_SENSE

C7A6 10PF 5% 50V 603 EMPTY

41 IN AUD_MIC2

R7A282 0 5% 402 EMPTY

AUD_MIC2_IN

UNSTUFF FOR 4205_PLL ONLY

R9A18 0 5% 402 CH

VCC3

C9A32 1UF 20% 16V Y5V 402

C9A34 4.7UF 20% 16V Y5V 1206

C9A31 1UF 20% 16V Y5V 402

STUFF FOR 4205_PLL ONLY

R9A17 0 5% EMPTY 402

AUD_A_REFFLT OUT 39

AUD_A_VREF OUT 39

AUD_AFLT1 OUT 39

AUD_AFLT2 OUT 39

AUD_AFLT3 OUT 39

AUD_AFLT4 OUT 39

AUD_3D_R OUT 39

AVDD3_ANALOG_R OUT 44

AVSS3_GNDSTRAP OUT 44

45 IN V_5P0_AUD_ANALOG

C9A13 10.0UF 10% 10V Y5V 603

C9A14 1UF 20% 16V Y5V 402

AVSS2_DCPL

C9A21 10.0UF 10% 10V Y5V EMPTY 603

STUFF:
4201 = 1UF
4205 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

R9A10 0 5% CH 402

STUFF:
4201/05 = EMPTY
9766 = 0 OHM
1885/86 = 0 OHM
1981 = 0 OHM

R9A14 0 5% CH 402

R9A13 0 5% CH 402

STUFF:
4201/05 = EMPTY
9766 = 0 OHM
1885/86 = 0 OHM
1981 = 0 OHM

STUFF FOR VV BOARD
EMPTY ON PRODUCTION BOARD
FOR NON ADI CODECS

V_5P0_AUD_ANALOG IN 45

C9A24 1.0UF 10% 10V Y5V 603

C9A25 1UF 20% 16V Y5V 402

45 IN V_5P0_AUD_ANALOG

C9A18 1.0UF 10% 10V Y5V 603

C9A20 1UF 20% 16V Y5V 402

STUFF:
4201/05 = 1UF
9766 = 1UF
1885/86 = 1UF
1981 = 1UF

STUFF:
4201/05 = .1UF
9766 = .1UF
1885/86 = .1UF
1981 = .1UF

DEFAULT STUFFING ADI 1981

AUDIO CODEC

SUPPORTS:
AD1885/86, AD1981,
CS4205, STAC9766

DRAWING
FAB_A.SCH.1.38
Mon Nov 18 12:47:11 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	38	4.0

KEEP CAPS AS CLOSE AS POSSIBLE TO AC97 CODEC.

38 IN AUD_A_REFFLT

38 IN AUD_A_VREF

STUFF:
4201/05 = .1UF
9766 = EMPTY
1885/86 = .1UF
1981 = EMPTY

C9A12
1UF
20%
16V
EMPTY
402

STUFF:
4201/05 = EMPTY
9766 = EMPTY
1885/86 = 10UF
1981 = 10UF

C9A1
10UF
20%
35V
EMPTY
RDL

38 IN AUD_AFLT1
38 IN AUD_AFLT2
38 IN AUD_AFLT3
38 IN AUD_AFLT4

38 IN AUD_3D_R

38 IN AUD_3D_C

C9A17
.1UF 20%
16V
EMPTY
402

STUFF:
4201 = 1000PF
4205 = EMPTY
9766 = EMPTY
1885/86 = .1UF
1981 = EMPTY

C9A16
.047UF
10%
10V
EMPTY
402

STUFF:
4201/05 = EMPTY
9766 = EMPTY
1885/86 = .047UF
1981 = EMPTY

R9A2
0
5%
EMPTY
402

STUFF:
4201 = 0 OHM
4205 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

C9A9
1UF
10%
10V
EMPTY
805

STUFF:
4201/05 = 2.2UF
9766 = 1UF
1885/86 = EMPTY
1981 = EMPTY

STUFF:
4201 = .01UF
4205 = EMPTY
9766 = .1UF
1885/86 = .1UF
1981 = EMPTY

C9A6
.1UF
10%
16V
EMPTY
402

C9A4
270PF
5%
50V
NP0
603

STUFF:
4201 = 1UF
4205 = EMPTY
9766 = 1UF
1885/86 = 1UF
1981 = 270PF

C9A10
270PF
5%
50V
NP0
603

STUFF:
4201 = EMPTY
4205 = 1000PF
9766 = EMPTY
1885/86 = 1UF
1981 = 270PF

C9A11
270PF
5%
50V
NP0
603

C9A3
270PF
5%
50V
NP0
603

STUFF:
4201/05 = 1000PF
9766 = 470PF
1885/86 = 270PF
1981 = 270PF

C9A2
1UF
10%
6.3V
X5R
402

STUFF:
4201/05 = .1UF
9766 = .1UF
1885/86 = .1UF
1981 = .1UF

DEFAULT STUFFING ADI 1981

CODEC FILTER CAPS: 1981, 1885/86, 4205, 9766

AUDIO SUBMODULE 2

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE41] [MOD_REV=REV0_60C] [PAGE_TITLE=CODEC] [LAST_MAKEGOLD: 6/14/99 9:20:55am]

DRAWING FAB_A.SCH.1.39
Mon Nov 18 12:47:20 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	39	4.0

[DONOR_REV=1.02/page40] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page39] [PROJ_NAME=_____G_DDR--1164] [LAST_MAKEPROJ: 10/12/2001 1:56:58 PM]

[FULL_ID=1164-44-1[illegible] [PAGE_INFO_ID=16476] [MODULE_ID=128-42-1[illegible] [DONOR_ID=1130-41-152081]

AUX IN

ATAPI HEADER

J6B1
1X4HDR
WHITE

AUD_LAUXIN_R — RP9A3 6.8K SM 5%.25W IC — AUD_LAUXIN_C — C9A29 X5R 1UF 20% 6.3V 603 — AUD_LAUXIN — OUT 38

AUD_RAUXIN_R — RP9A3 6.8K SM 5%.25W IC — AUD_RAUXIN_C — C9A30 X5R 1UF 20% 6.3V 603 — AUD_RAUXIN — OUT 38

RP9A3 6.8K 5% .25W IC SM (pin 6)

RP9A3 6.8K 5% .25W IC SM (pin 7)

CD IN

ATAPI HEADER

J6B2
1X4HDR
BLACK

AUD_LCD_R — RP9A2 6.8K SM 5%.25W IC — AUD_LCD_C — C9A28 X5R 1UF 20% 6.3V 603 — AUD_LCD — OUT 38

AUD_CDGND_R — RP8A1 6.8K SM 5%.25W IC — AUD_CDGND_C — C9A27 X5R 1UF 20% 6.3V 603 — AUD_CDGND — OUT 38

RP8A1 2 — 6.8K SM 5%.25W IC — 7

AUD_RCD_R — RP9A2 4 — 6.8K SM 5%.25W IC — RP9A2 5 — AUD_RCD_C — C9A26 X5R 1UF 20% 6.3V 603 — AUD_RCD — OUT 38

RP9A2 6.8K 5% .25W IC SM (pin 7)

RP9A2 6.8K 5% .25W IC SM (pin 6)

RP8A1 6.8K 5% .25W IC SM (pin 6)

RP8A1 6.8K 5% .25W IC SM (pin 5)

J6A1
3 STACK AUDIOJACK
JACK

AUD_RLINEIN_R — 0.2A FB6A6 FB — AUD_RLINEIN_R_FB — RP9A1 4 — 6.8K SM 5%.25W IC — AUD_RLINEIN_C — C9A19 X5R 1UF 20% 6.3V 603 — AUD_RLINEIN — OUT 38

AUD_LLINEIN_R — FB6A5 FB 0.2A — AUD_LLINEIN_R_FB — RP9A1 1 — 6.8K SM 5%.25W IC — AUD_LLINEIN_C — C9A22 X5R 1UF 20% 6.3V 603 — AUD_LLINEIN — OUT 38

C6A6 220PF 10% 50V X7R 402

C6A7 220PF 10% 50V X7R 402

RP9A1 6.8K 5% .25W IC SM (pin 7)

RP9A1 6.8K 5% .25W IC SM (pin 6)

45 42 41 OUT AUD_JACK_GND

TELEPHONY

ATAPI HEADER

J8B1
1X4HDR
HDR
GREEN
NC=5

R8A6 2 — 1K 402 1% CH — 1

AUD_PHONE_CONN — R8A4 1K 1% EMPTY 402 — 2

AUD_PHONE_C — C8A7 1.0UF 10% 10V X5R 603 — AUD_PHONE — OUT 38

AUD_MONO_OUT — C8A6 1.0UF 10% 10V X5R 603 — IN 38

AUD_MONO_OUT_C — OUT 43

AUDIO SUBMODULE 5

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE27] [MOD_REV=REV0_60C]
[PAGE_TITLE=ATX_ATAPI_CONNECTORS] [LAST_MAKEGOLD: 6/14/99 9:19:23am]
DRAWING FAB_A.SCH.1.40 Mon Nov 18 13:50:34 2002 D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	40	4.0

MIC IN, DISCRETE PINK
MONO CONN

J6A1
3 STACK AUDIOJACK

JACK

CAD NOTE:
VOID GRND PLANE
CONNECT THICK TRACE
TO GROUND ON AUDIO_NET

NEAR CONN

45 42 40 OUT AUD_JACK_GND

NET_AUD_MICIN_P5

C6A3 470PF 10% 50V X7R 402

C6A2 470PF 10% 50V X7R 402

NET_AUD_MICIN_P2

FB6A1 FB

600 0.2A BROAD

FB6A2 FB

NET_AUD_MICIN_FB

AUD_MIC_AMP

STUFF
MIC = 4.7K
SPDIF = 110 OHM

R7A13 110 1% CH 402

STUFF
MIC = 1UF
SPDIF = EMPTY

C7A1 1.0UF 10% 10V Y5V EMPTY 603

R7A22 4.7K 5% EMPTY 402

R7A24 22K 5% CH 402

R7A20 0 5% EMPTY 402

38 OUT AUD_MIC_IN

C9A23 1.0UF 10% 10V Y5V 603

AUD_MIC_IN_AMPOUT_PN1

44 43 OUT AUD_MIC_BIAS

NEAR AMP
AUD_MIC_AMP
R7A191 2.2K 5% 402 CH

NEAR AMP
R7A101 2.2K 5% 402 EMPTY

STUFF
MIC = 2.2K
SPDIF = EMPTY

AUD_MIC_AMP
U7A1 LF353
IC

AUD_MIC_BIAS_REF

AUD_MIC_BIAS_R

R7A33 2.2K 5% CH 402

C7A4 1.0UF 10% 10V EMPTY 603

AUD_MIC_AMP
R7A271 4.7K 5% 402 CH

C7A7 1.0UF 10% 10V Y5V 603

AUD_MIC_IN_FP IN 43

NEAR AMP
R7A252 10K 5% 402 CH

V_5P0_AUD_ANALOG IN 45

C7A5 1.0UF 10% 10V Y5V 603

AUD_MIC_AMP

AUD_MICIN_AMP_PLUS

AUD_SPDIF_MIC IN 42

+12V

NEAR AMP
R7A5 10 5% CH 402

V_P12V_R

C7A3 1UF 20% 16V Y5V 402

U7A1 LF353
IC

V_N12V_R

NEAR AMP
R7A26 10 5% CH 402

C7A8 1UF 20% 16V Y5V 402

-12V

AUD_MICIN_AMP_MINUS

C7A2 47PF 5% 50V C0G 402

AUD_MIC_IN_AMPOUT_PN2

R7A4 2 100K 5% 402 CH

STUFF
4201 = 0 OHM
4205 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = EMPTY

R7A9 2 0 5% 402 EMPTY

R7A122 1K 5% 402 CH

R7A16 220 5% CH 402

R7A6 4.7K 5% CH 402

R8A5 4.7K 5% CH 402

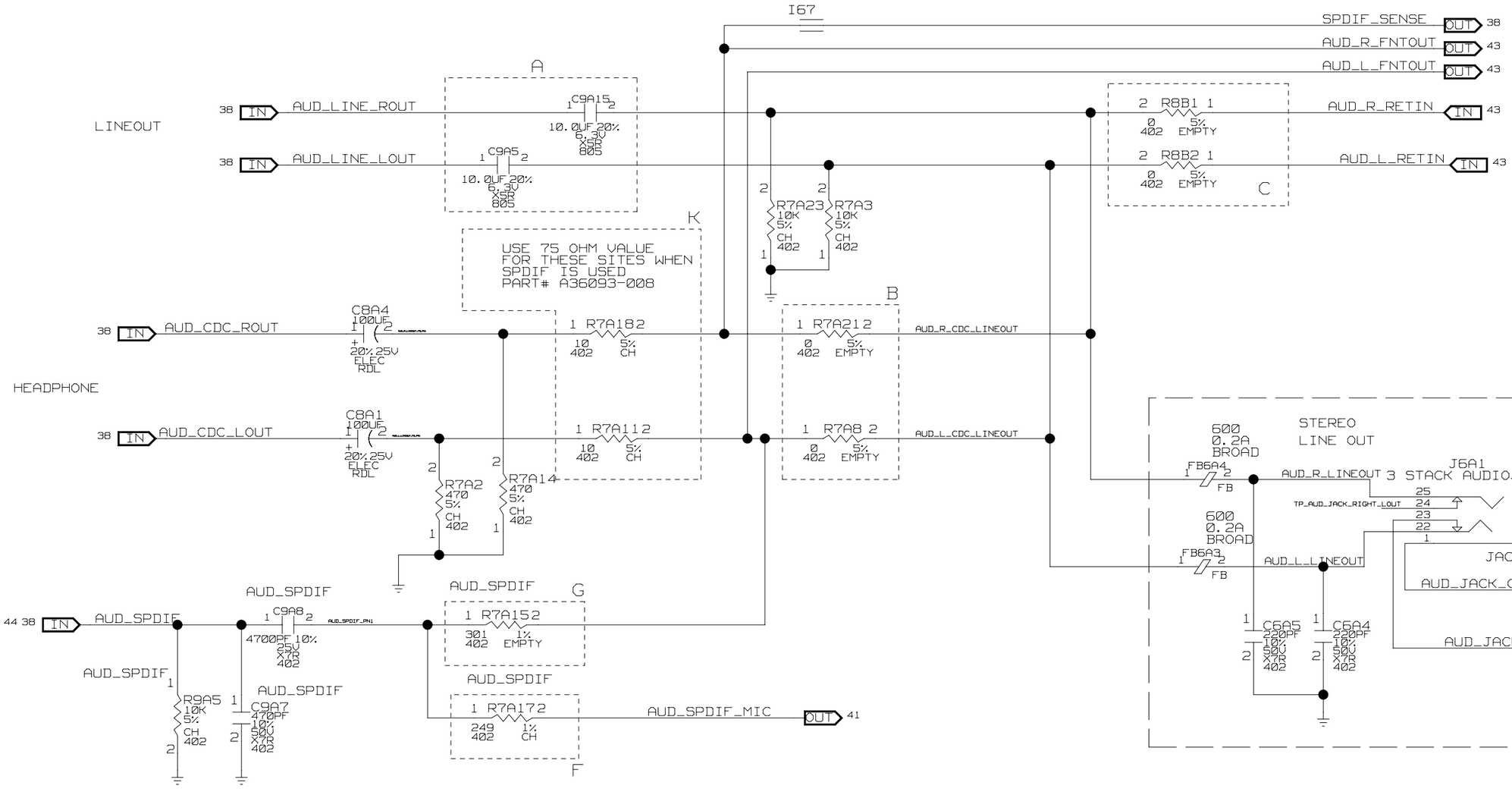
AUD_MIC2 OUT 38

AUDIO SUBMODULE 4

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE33] [MOD_REV=REV0_60C] [PAGE_TITLE=ATX_MIC_PREAMP&OUTAMP_FB]

DRAWING
FAB_A.SCH.1.41
Mon Nov 18 12:28:45 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	41	4.0



	BP ONLY	FP--> BP
HEADPHONE	STUFF B EMPTY A, C	STUFF C EMPTY A, B
LINEOUT	STUFF A EMPTY B, C	N/A

SPDIF	BP LO	BP MIC
F	EMPTY	STUFF
G	STUFF	EMPTY
H	EMPTY	110 OHM
J	STUFF	EMPTY
K	75 OHM	10 OHM

AUDIO SUBMODULE 3

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE36] [MOD_REV=REV0_60C]
[PAGE_TITLE=TDA1308/LM4880_AMP]
[LAST_MAKEGOLD: 6/14/99 9:20:13am]

DRAWING
FAB_A.SCH.1.42
Mon Nov 18 13:50:42 2002
D845GFT FAB_A

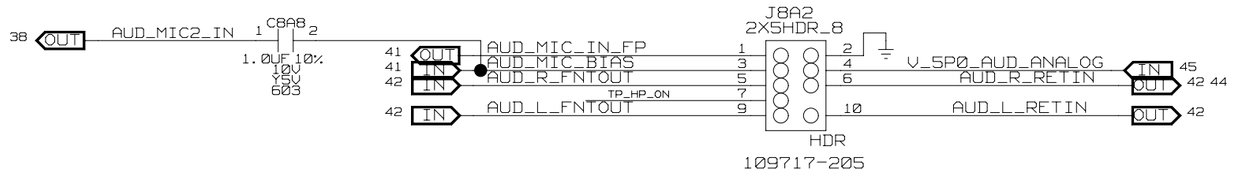
DOCUMENT NUMBER	PAGE	REV
C23021	42	4.0

[DONOR_REV=1.02/page43]
[DONOR_PROJ=NBVV_DDR--1130]
[PROJ_REV=2.00/page42]
[PROJ_NAME= _G_DDR--1164]
[LAST_MAKEPROJ: 10/12/2001 1:56:59 PM]

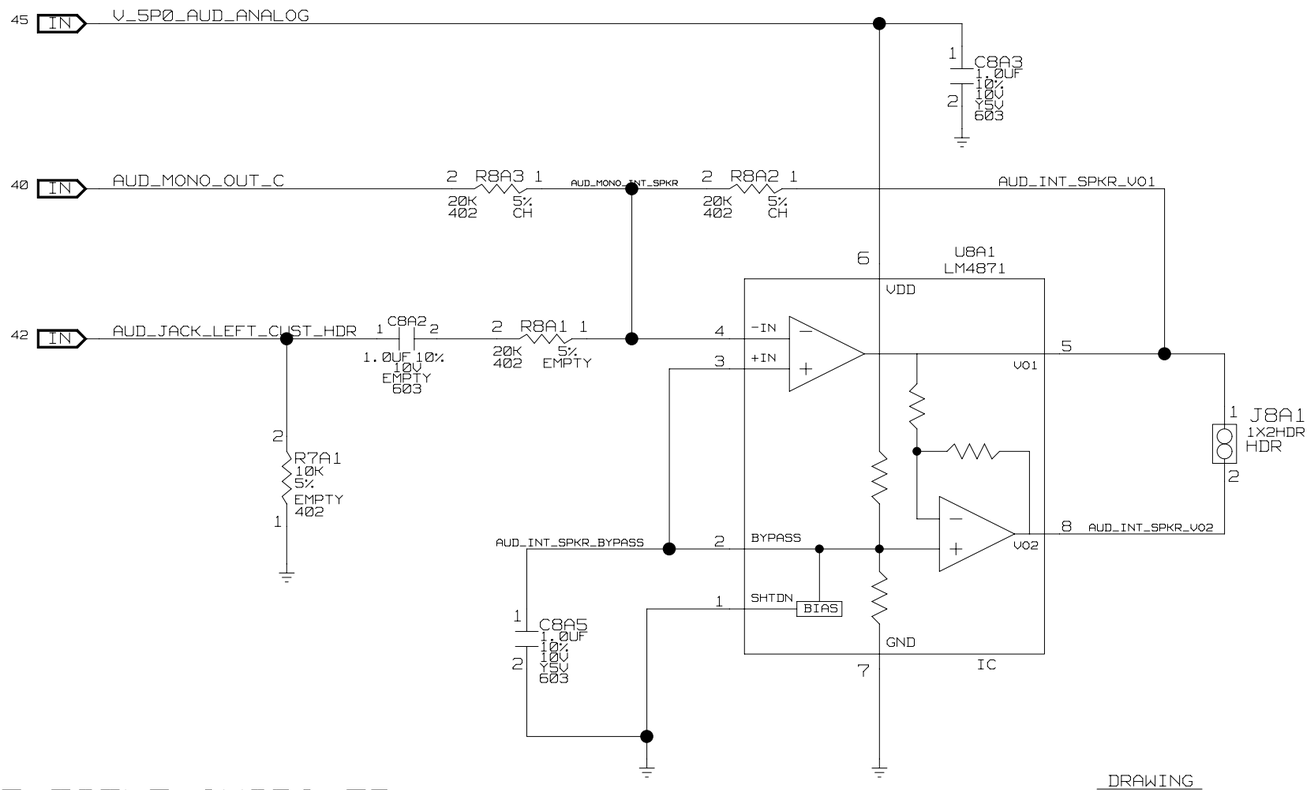
NOTE:
ADD EMI CAPS

NOTE:
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION

AUDIO FRONT PANEL
PLACE NEAR AUDIO CIRCUIT



INTERNAL SPEAKER CIRCUIT



[PAGE_TITLE=AUIDO_FP]

DRAWING
FAB_A.SCH.1.43
Mon Nov 18 12:29:03 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	43	4.0

MIC JACK SENSE

GPIO LOCATIONS:

NOT CONNECTED

4205: 43, 44, 41, 40, 39
1981: 16, 17 (ACTIVE HIGH)
9766: 43, 44
4291: NONE
1885/86: 47, 48

45 IN V_5P0_AUD_ANALOG

R9B10 47K 5% CH 402
R9B12 47K 5% CH 402

AUD_MIC_JS

R9B11 2K 5% 402 CH

NOTE:
SHOULD BE
1K OHM

AUD_MIC_BIAS_JS_R

Q9B1
MBT3904DUAL

41 IN AUD_MIC_BIAS

R9B9 10K 5% 402 CH

AUD_MIC_JS_R

XSTR

TOP

R9A7 0 5% 402 CH — AUD_CODEC_16 — OUT 38

R9A9 0 5% 402 EMPTY — AVSS3_GNDSTRAP — OUT 38

R9A122 0 5% 402 EMPTY — AUD_SPDIF — OUT 38 42

NOTE:
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

R9B7 2.2K 5% 402 CH

AUD_R_RETIN_HD_PH_JS

STUFF
4201/05 = EMPTY
9766 = EMPTY
1885/86 = EMPTY
1981 = 2.2K

HEADPHONE JACK SENSE

CHANGE TO
201036-002

201036-001
CR9B1

43 IN AUD_R_RETIN

GP SOT23S EMPTY

R9B1 2.2K 5% 402 EMPTY

AUD_HD_PH_JS

C9B3 2.2UF 20% 10V EMPTY 805

TOP

R9A6 0 5% 402 CH — AUD_CODEC_17 — OUT 38

R9A8 0 5% 402 EMPTY — AVDD3_ANALOG_R — OUT 38

R9A112 0 5% 402 EMPTY — AUD_JS0 — OUT 38

NOTE:
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

STUFF
4201/05 = STUFF
9766 = STUFF
1885/86 = STUFF
1981 = EMPTY

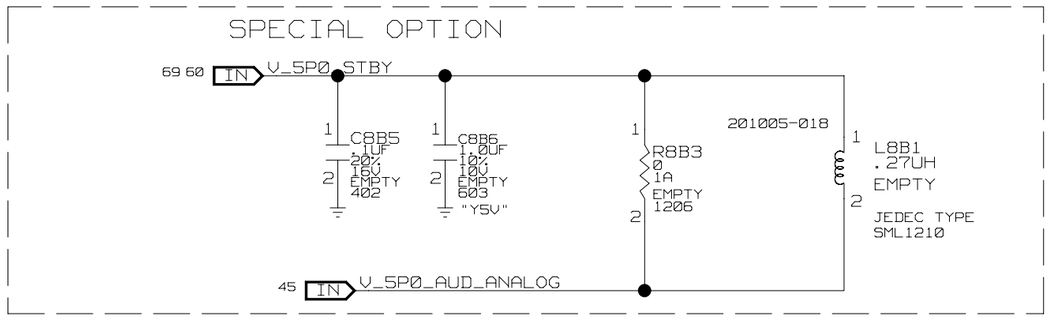
DEFUALT
STUFFING
ADI 1981

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE38] [MOD_REV=REV0_60C] [PAGE_TITLE=TRANSIENT] [LAST_MAKEGOLD: 6/14/99 9:20:22am]

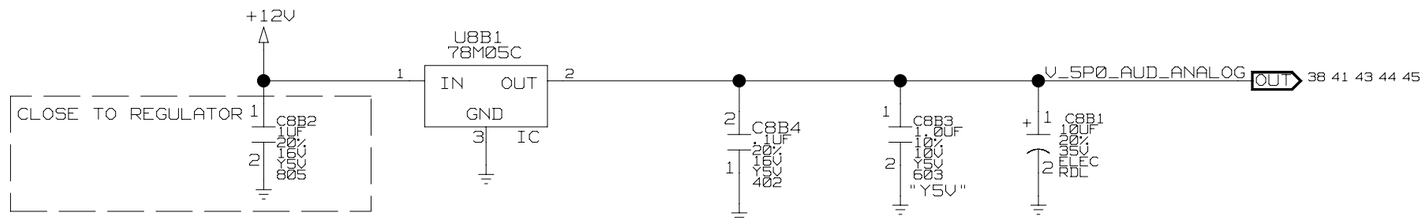
DRAWING FAB_A.SCH.1.44
Mon Nov 18 12:29:11 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	44	4.0

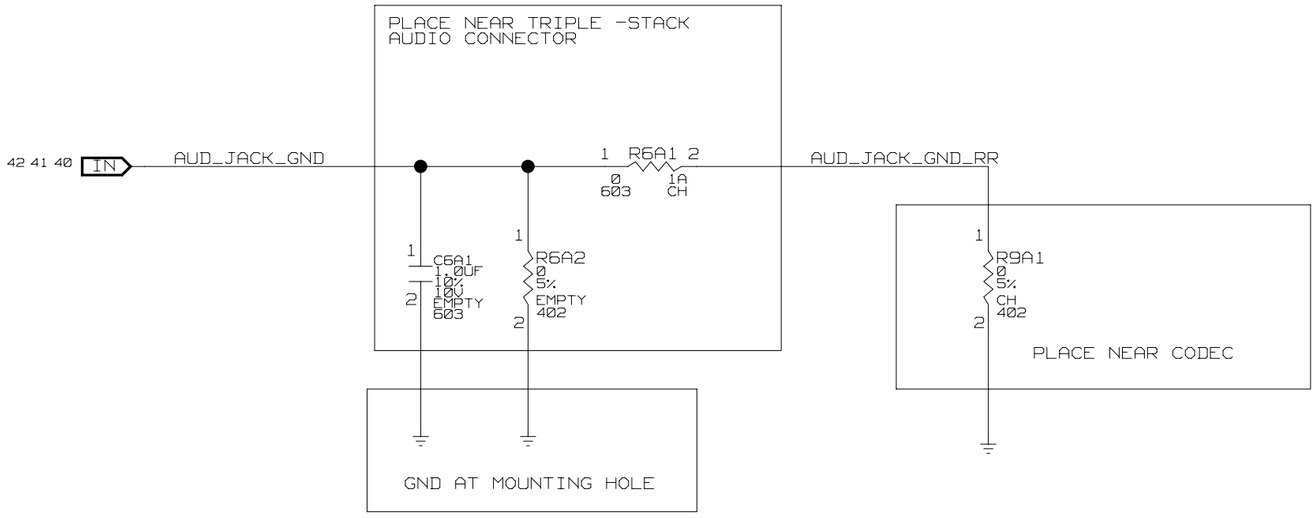
[DONOR_REV=1.02/page45] [DONOR_PROJ=NBVV_DDR--1130]
[PROJ_REV=2.00/page44] [PROJ_NAME= :_G_DDR--1164]
[LAST_MAKEPROJ: 10/12/2001 1:57:00 PM]



REGULATOR THERMAL TAB SHOULD BE SOLDERED TO A COPPER PAD THAT IS LARGE ENOUGH TO ALLOW 5 TO 10 GROUND VIAS AROUND THE COMPONENT FOR COOLING



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO V_5P0_AUD_ANALOG



[PAGE_TITLE=AUDIO_VREG]

DRAWING FAB_A.SCH.1.45
Mon Nov 18 12:29:21 2002
D845GFT FAB A

	DOCUMENT NUMBER	PAGE	REV
	C23021	45	4.0

[SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE34] [MOD_REV=REV0_60C] [LAST_MAKEGOLD: 6/14/99 9:19:58am]

SPARE SECTIONS

TP_RP10_10000_4

RP1H1 10K 5% .063W IC SM (4 / 5) TP_RP10_10000_5

U1H1
LPC47M102

69 63 IN V_3P3_STBY

RP1H1 10K 5% .063W IC SM (2 / 7) → 24 OUT IO_PME*

VCC3

RP1H2 10K 5% .063W IC SM (2 / 7)

RP1H2 10K 5% .063W IC SM (1 / 8)

24 OUT L_DRQ*
69 25 IN P_PCIRST*
72 24 BI SER_IRQ

R1H8 0 603 1A CH

VCC3

RP1H1 10K 5% .063W IC SM (3 / 6)

FLOPPY

47 OUT	SIO_FDD_DRVDEN0	1	DRVDEN0/GP40
47 OUT	SIO_FDD_DRVDEN1	2	DRVDEN1/GP41
47 OUT	SIO_FDD_MTR0*	3	MTR0
47 OUT	SIO_FDD_DS0*	5	DS0
47 OUT	SIO_FDD_DIR*	8	DIR
47 OUT	SIO_FDD_STEP*	9	STEP
47 OUT	SIO_FDD_WDATA*	10	WDATA
47 OUT	SIO_FDD_WGATE*	11	WGATE
47 OUT	SIO_FDD_HDSEL*	12	HDSEL
47 IN	SIO_FDD_INDEX*	13	INDEX
47 IN	SIO_FDD_TRK0*	14	TRK0
47 IN	SIO_FDD_WRTPRT*	15	WRTPRT
47 IN	SIO_FDD_RDATA*	16	RDATA
47 IN	SIO_FDD_DSKCHG*	4	DSKCHG

LPC

		17	IOPME*/GP42
75 51 24 BI	L_AD<3..0>	20 / 21 / 22 / 23	AD0 / AD1 / AD2 / AD3
24 IN	L_FRAME*	24	FRAME
		25	DRQ
	SIO_PCI_RST*	26	PCI_RESET
	L_PD*	27	PD
69 7 IN	CK_P_33M_SIO	29	PCI_CLK
		30	SER_IRQ

SERIAL 1

50 IN	SIO_COM_RXD1	84	RXD1
50 OUT	SIO_COM_TXD1	85	TXD1
50 IN	SIO_COM_DSR1*	86	DSR1
50 OUT	SIO_COM_RTS1*	87	RTS1
50 IN	SIO_COM_CTS1*	88	CTS1
50 OUT	SIO_COM_DTR1*	89	DTR1
50 IN	SIO_COM_RI1*	90	RI1
50 IN	SIO_COM_DCD1*	91	DCD1

NOTE:
BIOS TO PROGRAM
AS OUTPUTS
1

SERIAL 2 /GPIO

TP_SIO_COM_RI2*		92	GP50/R12*
TP_SIO_COM_DCD2*		94	GP51/DCD2*
TP_SIO_COM_RXD2		95	GP52/RXD2/IRRX
TP_SIO_COM_TXD2		96	GP53/TXD2/IRTX
TP_SIO_COM_DSR2*		97	GP54/DSR2*
TP_SIO_COM_RTS2*		98	GP55/RTS2*
TP_SIO_COM_CTS2*		99	GP56/CTS2*
TP_SIO_COM_DTR2*		100	GP57/DTR2*

VCC → 44 VREF

1 C1H3 1UF 20% 25VC 603 2

69 63 IN V_3P3_STBY → 18 VTR

40 AVSS

VCC3=53,65,93
GND=7,31,60,76

IC

JOY

GP10/J1B1	32	TP_SIO_GAME_J1B1	
GP11/J1B2	33	TP_SIO_GAME_J1B2	
GP12/J2B1	34	TP_SIO_GAME_J2B1	
GP13/J2B2	35	TP_SIO_GAME_J2B2	
GP14/J1X	36	TP_SIO_GAME_J1X	
GP15/J1Y	37	TP_GP15	
GP16/J2X	38	TP_GP16	# 1
GP17/J2Y	39	TP_SIO_39	
GP25/MIDI_IN	46	TP_SIO_46	
GP26/MIDI_OUT	47	TP_SIO_GP26	

GPIO

P17/GP20	41	GP20_STRAP	IN 77
P16/GP21	42	GP21_STRAP	IN 77
P12/GP22	43	TP_SIO_GP22	
SYSOPT/GP24	45	SIO_GP24	
LED1/GP60	48	TP_SIO_GP60	
LED2/GP61	49	TP_SIO_GP61	
IO5MI*/GP27	50	IO_SMI*	OUT 24
FDC_PP/DDRC/GP43	28	TP_SIO_GP43	# 1

KEY/MOUSE

KDAT	56	SIO_KBDATA	BI 48
KCLK	57	SIO_KBCLOCK	BI 48
MDAT	58	SIO_MSDATA	BI 48
MCLK	59	SIO_MSCLOCK	BI 48
GP36/KBDRST	63	KBRST*	
GP37/A20M	64	A20GATE	

PARALLEL

INIT	66	SIO_LPT_INIT*	BI 49
SLCTIN	67	SIO_LPT_SLCTIN*	OUT 49
PD0	68	0	
PD1	69	1	
PD2	70	2	
PD3	71	3	
PD4	72	4	
PD5	73	5	
PD6	74	6	
PD7	75	7	SIO_LPT_PD<7..0> BI 49
SLCT	77	SIO_LPT_SLCT	IN 49
PE	78	SIO_LPT_PE	IN 49
BUSY	79	SIO_LPT_BUSY	IN 49
ACK	80	SIO_LPT_ACK*	IN 49
ERR	81	SIO_LPT_ERR*	IN 49
ALF	82	SIO_LPT_ALF*	OUT 49
STROBE	83	SIO_LPT_STROBE*	OUT 49

IR

IRRX2/GP34	61	SIO_IRRX2	IN 55
IRTX2/GP35	62	SIO_IRTX2	OUT 55

FAN

GP32/FAN2	54	TP_SIO_FAN2_PWM	
GP33/FAN1	55	FAN1_PWM	
FAN_TACH2/GP30	51	FRONT_FAN_TACH	IN 57
FAN_TACH1/GP31	52	REAR_FAN_TACH	IN 57

CLOCK

CLOCKI	19	CK_14M_SIO	IN 7 69
CLKI32	6	SUSCLK	IN 24

69 63 IN V_3P3_STBY → RP1H1 10K 5% .063W IC SM (1 / 8)

BIOS DETECTS ADDRESS WITHOUT STUFFING

VCC3

R1H3 4.7K 5% EMPTY 603 (1 / 2)

R1H2 4.7K 5% CH 603 (1 / 2)

VCC3

RP1H2 10K 5% .063W IC SM (3 / 6)

RP1H2 10K 5% .063W IC SM (4 / 5)

OUT 24
OUT 24

† EMPTY IF HECETA6 IS STUFFED

R1H1 0 603 1A CH (1 / 2) FNT_REAR_FAN_PWM3 OUT 53 57

69 63 IN V_3P3_STBY

VCC3

C1H4 1UF 20% 25VC 603 (1 / 2)
C1H2 1UF 20% 25VC EMPTY 603 (1 / 2)
C2H2 1UF 20% 25VC 603 (1 / 2)
C1H1 1UF 20% 25VC 603 (1 / 2)

PLACE NEAR SMC DEVICE PINS 56,65,93,125

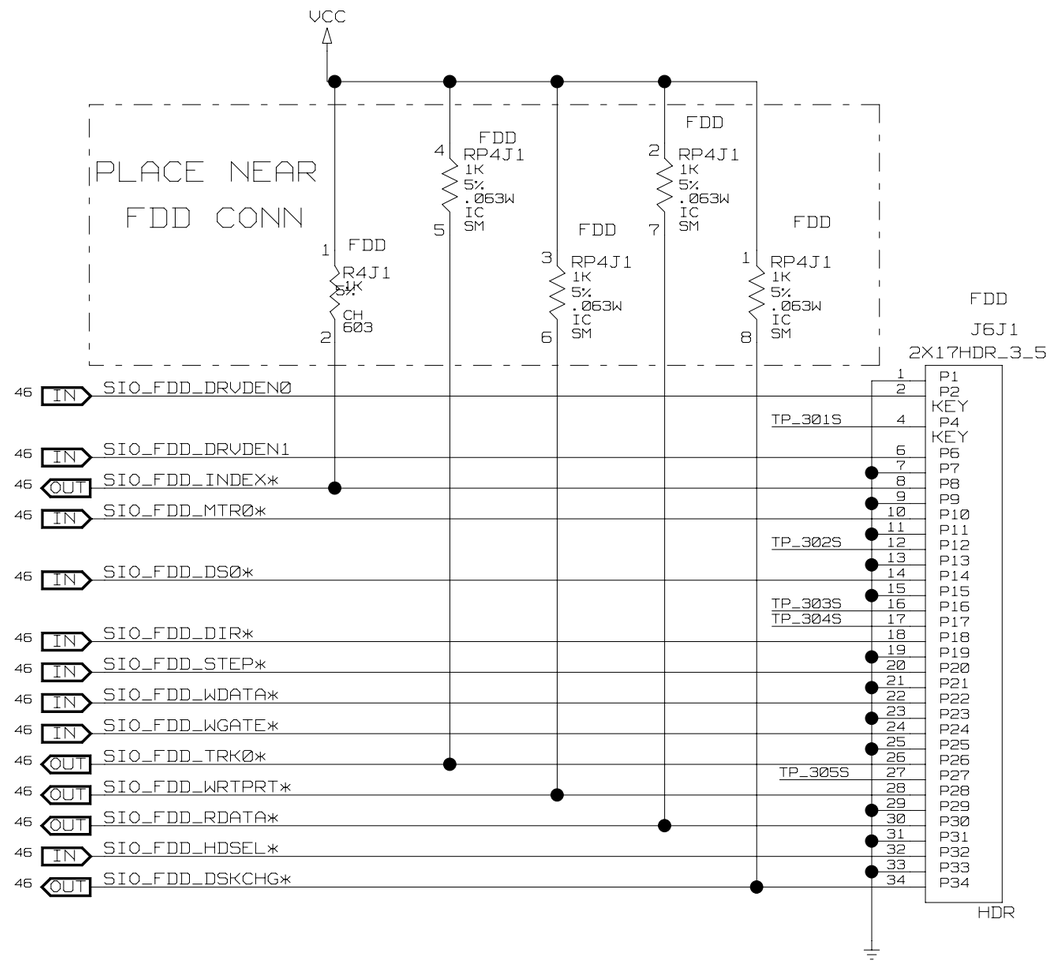
NOTE: #1
BIOS TO PROGRAM THESE
GPIO'S AS OUTPUTS

DRAWING
FAB_A.SCH.1.46
Mon Nov 18 13:50:51 2002
D845GFT FAB_A

[PAGE_TITLE=SIO_LPC_47MXXX]

DOCUMENT NUMBER	PAGE	REV
C23021	46	4.0

[FULL_ID=1164-51-164902] [PAGE_INFO_ID=164901] [MODULE_ID=128-49-14720] [DONOR_ID=1130-48-152221]



[PAGE_TITLE=ATX_FLOPPY]

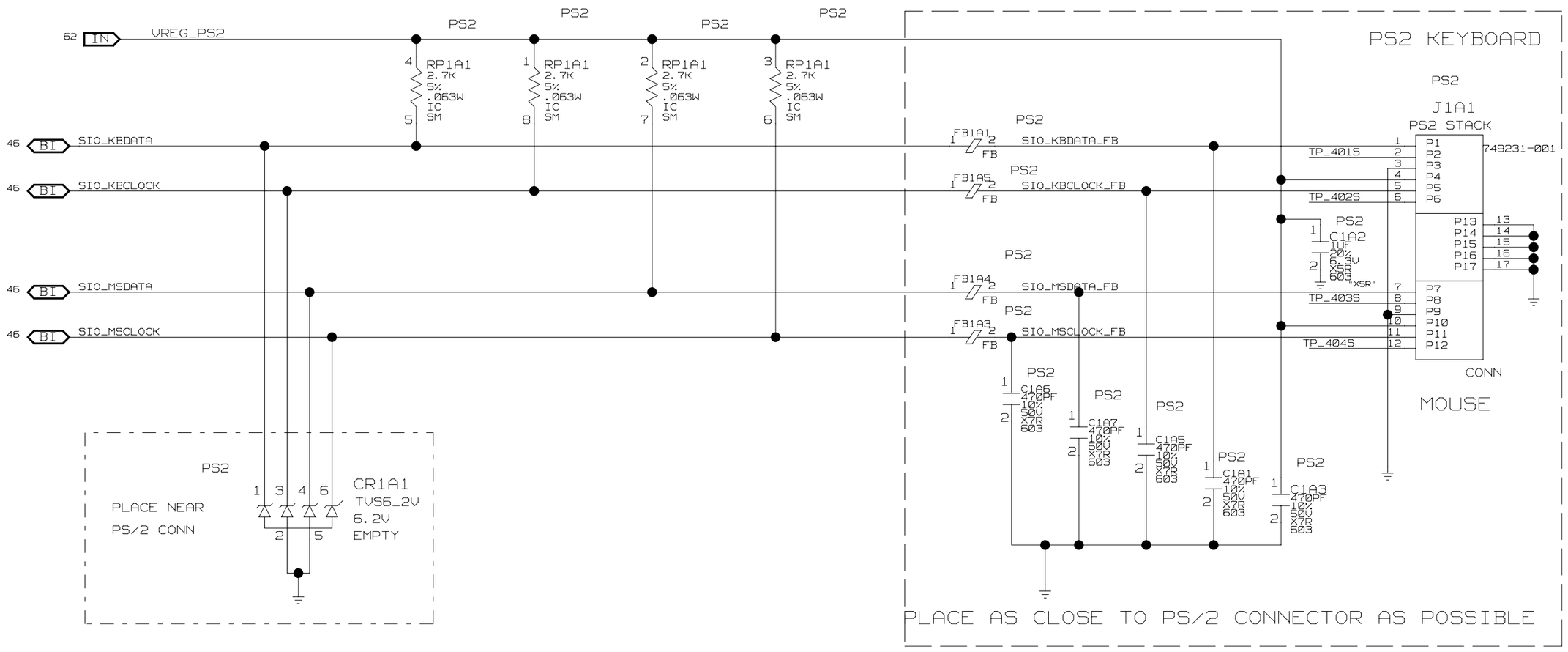
DRAWING
FAB_A.SCH.1.47
Mon Nov 18 13:51:00 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	47	4.0

[DONOR_REV=1.02/page48] [DONOR_PROJ=NBVV_DDR--1164] [MODULE=SIO]
[PROJ_REV=2.00/page47] [PROJ_NAME= _G_DDR--1164]
[SOLUTION=SMSC/LPC47B27X] [MOD_PAGE=PAGE3] [MOD_REV=REV0_91C]
[LAST_MAKEPROJ: 10/12/2001 1:57:01 PM]
[LAST_MAKEGOLD: 6/28/99 11:05:37am]

[FULL_ID=1164-52-16492] [PAGE_INFO_ID=16492] [MODULE_ID=128-50-1470] [DONOR_ID=1130-49-15224]

COMPONENTS ARE DFM29



ATX DOUBLE-STACKED

DRAWING
FAB_A.SCH.1.48
Mon Nov 18 13:51:09 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	48	4.0

[DONOR_REV=1.02/page49] [DONOR_PROJ=NBVV_DDR--1130] [MODULE=SIO]
[PROJ_REV=2.00/page48] [PROJ_NAME=_G_DDR--1164]
[MOD_PAGE=PAGE4] [MOD_REV=REV0.91C]
[PAGE_TITLE=PS2_KEYBOARD/MOUSE]
[LAST_MAKEGOLD: 5/28/99 11:05:40am]
[LAST_MAKEPROJ: 10/12/2001 1:57:02 PM]
[SOLUTION=SMSC/LPC47B27X]

COMPONENTS ARE DFM29

46 IN SIO_LPT_PD<7..0>

RP3A1 33 SM 5% .063W IC
- 6 → SIO_LPT_PD6_R
- 7 → SIO_LPT_PD7_R

RP4A1 33 SM 5% .063W IC
- 0 → SIO_LPT_PD0_R
- 1 → SIO_LPT_PD1_R
- 2 → SIO_LPT_PD2_R
- 3 → SIO_LPT_PD3_R

RP3A1 33 SM 5% .063W IC
- 4 → SIO_LPT_PD4_R
- 5 → SIO_LPT_PD5_R

VCC

RP4A2 2.7K 5% .063W IC SM
- 3 → 6
- 4 → 5
- 1 → 8
- 2 → 7

46 IN SIO_LPT_STROBE* → RP4A3 33 SM 5% .063W IC → SIO_LPT_STROBE_R*

46 IN SIO_LPT_ALF* → RP4A3 33 SM 5% .063W IC → SIO_LPT_ALF_R*

46 IN SIO_LPT_INIT* → RP4A3 33 SM 5% .063W IC → SIO_LPT_INIT_R*

46 IN SIO_LPT_SLCTIN* → RP4A3 33 SM 5% .063W IC → SIO_LPT_SLCTIN_R*

VCC

RP3A2 10K 5% .063W IC SM
- 1 → 8
- 2 → 7
- 3 → 6
- 4 → 5

R4A3 10K 5% CH 603
- 1 → 2

46 OUT SIO_LPT_ACK*
46 OUT SIO_LPT_BUSY
46 OUT SIO_LPT_PE
46 OUT SIO_LPT_SLCT
46 OUT SIO_LPT_ERR*

J4A2
TALL DSUB 25
749179-001

1	14	2	15	3	16	4	17	5	18	6	19	7	20
8	21	9	22	10	23	11	24	12	25	13			

DSUB
GND=26, 27, 28

C3A5 C3A1 C4A9 C4A7 C3A12 C3A2 C4A13 C4A11 C3A6 C3A3 C4A10 C4A6 C3A7 C3A4 C4A14 C4A12 C4A8
220PF 10% 50V X7R 603

PLACE NEAR
LPT CONN

DRAWING
FAB_A.SCH.1.49
Mon Nov 18 12:29:58 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	49	4.0

[FULL_ID=1164-54-164956] [PAGE_INFO_ID=16495] [MODULE_ID=128-52-14500] [DONOR_ID=1130-51-152281]

COMPONENTS ARE DFM29

DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS COM1
BASE P/N

U2A1
GD75232S 621111-103

SIO_COM_DCD1* 19 RY1 — RA1 2
SIO_COM_DSR1* 18 RY2 — RA2 3
SIO_COM_RXD1 17 RY3 — RA3 4
SIO_COM_CTS1* 14 RY4 — RA4 7
SIO_COM_RI1* 12 RY5 — RA5 9
SIO_COM_RTS1* 16 DA1 — DY1 5
SIO_COM_TXD1 15 DA2 — DY2 6
SIO_COM_DTR1* 13 DA3 — DY3 8
1 VDD+ — VDD- 10

NOTE DIRECTION IC

+12V
VCC=20
GND=11
VCC=V_5P0_STBY
-12V

COM1 C2A7 470PF 10% 50V CMPTY 603
COM1 C2A6 470PF 10% 50V CMPTY 603
COM1 C2A5 470PF 10% 50V CMPTY 603
COM1 C3A10 470PF 10% 50V CMPTY 603
COM1 C3A8 470PF 10% 50V CMPTY 603
COM1 C2A4 470PF 10% 50V CMPTY 603
COM1 C3A11 470PF 10% 50V CMPTY 603
COM1 C3A9 470PF 10% 50V CMPTY 603

SERIAL PORT A

COM1 J2A1
2 ROW
749218-001
DSUB

SIO_COM_DCD1_232 1
SIO_COM_DSR1_232 6
SIO_COM_RXD1_232* 2
SIO_COM_RTS1_232 7
SIO_COM_TXD1_232* 3
SIO_COM_CTS1_232 8
SIO_COM_DTR1_232 4
SIO_COM_RI1_232 9
5
10
11

+12V — COM1_DCPL 202341-002 C2D3 .1UF 50V CERAMIC 603
-12V — COM1_DCPL 202341-002 C2D8 .1UF 50V CERAMIC 603
V_5P0_STBY — IN 60 69
COM1_DCPL 202341-002 C2D2 .1UF 50V CERAMIC 603

PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY

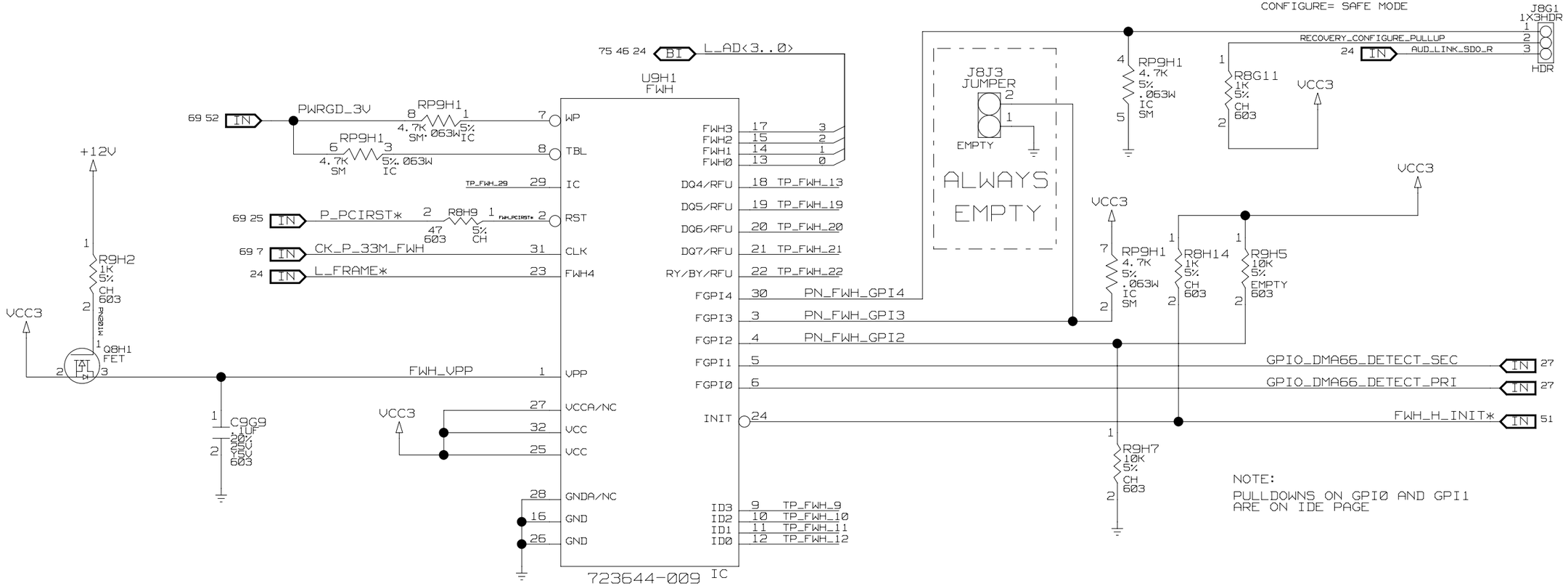
BOM=CORE_COM1

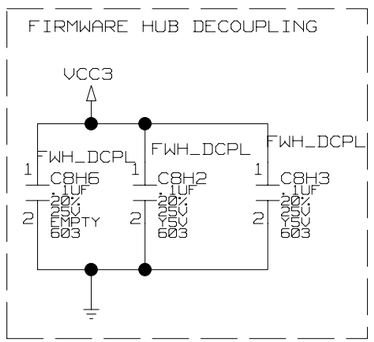
DRAWING
FAB_A.SCH.1.50
Mon Nov 18 12:30:07 2002
D845GFT FAB_A

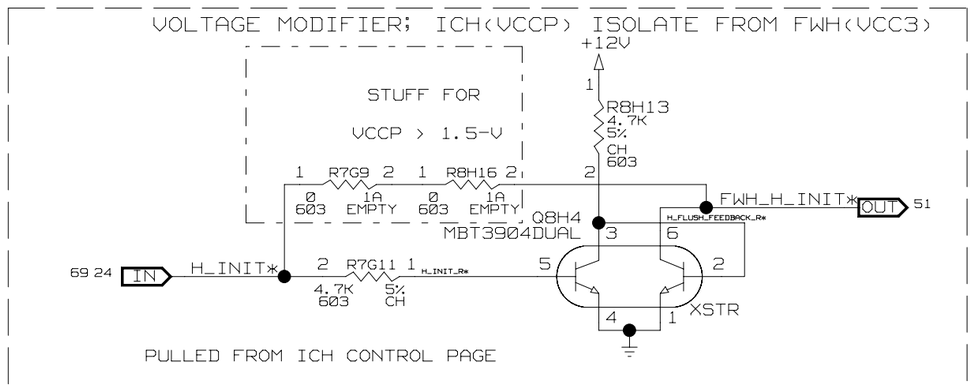
	DOCUMENT NUMBER	PAGE	REV
	C23021	50	4.0

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE







FIRMWARE HUB

DRAWING
FAB_A.SCH.1.51
Mon Nov 18 13:51:18 2002
[PAGE_TITLE=FIRMWARE_HUB] D845GFT FAB_A
[LAST_MAKEGOLD: 9/10/99 1:12:46pm]

	DOCUMENT NUMBER	PAGE	REV
	C23021	51	4.0

[MODULE=FWH] [SOLUTION=INTEL/FWH1_82802AC] [MOD_PAGE=PAGE2] [MOD_REV=REV2_0C]
[DONOR_REV=1.02/page52] [DONOR_PROJ=NBVV_DDR--1130]
[PROJ_REV=2.00/page51] [PROJ_NAME= :_G_DDR--1164]
[LAST_MAKEPROJ: 10/12/2001 1:57:03 PM]

GLUECHIP4

69 60 IN V_5P0_STBY
69 63 IN V_3P3_STBY
60 IN PWRGD_PS

C2J1 1UF 20% 25VC Y5VC 603
C2J4 1UF 20% 25VC Y5VC 603
C2J3 1UF 20% 25V Y5V 603

VCC3 RP2J2 1K 5% .063W IC SM
GLUE4_6_PU OUT 52
GLUE4_5_PU OUT 52
GLUE4_4_PU OUT 52

52 IN P_RST_SLOTS_R* — R2J4 33 603 5% CH — P_RST_SLOTS* OUT 21 69 31 32 33
C1J2 47PF 5% 50V NPO 603

69 60 IN V_5P0_STBY — R2J3 10K 5% CH 603

74 55 53 IN FP_RST* — R2G4 0 603 EMPTY 1A — R1J1 330 603 5% CH — GLUE_FP_RST_R* OUT 52
R2H11 0 1A CH 603
C1H5 1.0UF 10% 10V Y5V 603
71 69 8 IN H_DBR* — R2H10 0 603 EMPTY 1A

SCSI ACTIVITY LED

J9G1 107555-102 1X2HDR HDR
1 SCSI_ACT* OUT 52
2 TP_SCSI_ACT_PIN2

SPARES

TP_RP_THERM_10K_4 — RP2J1 10K 5% .063W IC SM — TP_RP_THERM_10K_5
RP2J2 1K 5% .063W IC SM

74 IN GLUE_SLOTOCC*
69 8 IN H_SKTOCC* — R2J5 33 603 5% EMPTY
NOTE: DEBUG ONLY

VCC3 — R1J7 2.7K 5% CH 603 — R1J6 2.7K 5% CH 603

52 R9G2 1 0 603 EMPTY 1A
52 IN RSMRST* — Q9G1 MMBT3906 XSTR — ICH_RSMRST* OUT 24
R8G6 10K 5% CH 603
R9G6 0 1A EMPTY 603
CR9G1 BAV99 SOT23S DIO
CR9F1 BAV99 SOT23S DIO
R9G3 2.2K 5% CH 603

69 63 IN V_3P3_STBY
RP1J1 1K 5% .063W IC SM
RP2J1 10K 5% .063W IC SM
RP2J1 10K 5% .063W IC SM

VCC VCC3

U2J1 GLUECHIP4 A12878-002 IC

52 IN	GLUE4_4_PU	4	GPO_FLUSH_CACHE/GP2_IN	VREF5IN	45
52 IN	GLUE4_6_PU	6	INIT/GP1_INA	VREF3IN	1
69 25 IN	P_PCIRST*	12	PCIRST	V_5P0_STBY	2
69 13 B IN	GLUE4_DDCSCL_3V	17	3V_DDCSCL	V_3P3_STBY	3
69 7 IN	CK_66M_GLUE	9	CLK_IN	REF5V	44
		21	CPU_PRESENT	HD_LED	24
27 IN	IDE_PRI_ACT*	25	PRIMARY_HD	PCIRST_OUT	13
52 IN	SCSI_ACT*	26	SCSI	AUD_RST	15
27 IN	IDE_SEC_ACT*	27	SECONDARY_HD	MUTE_AUD	46
TP_GLUE4_AUD_EN		14	AUD_EN	SCK_BJT_GATE	35
TP_MUTE_AUD*		47	AUD_SHDN	FLUSH_OUT_FWH	31
TP_GLUE4_TESTEN_41		41	TEST_EN	FLUSH_OUT_CPU/GP1_OUT	7
GLUE4_SEL_33_66_R		10	SEL_33_66	INIT_OUT/GP2_OUT	8
22 B IN	GLUE4_DDCSDA_5V	20	5V_DDCSDA	IDE_RSTDRV	16
60 IN	PWRGD_PS	32	PWRGD_PS	BACKFEED_CUT	28
69 13 B IN	GLUE4_DDCSDA_3V	19	3V_DDCSDA	LATCHED_BACKFEED_CUT	30
52 IN	GLUE_FP_RST_R*	33	FPRST	PWRGD_3V	34
22 B IN	GLUE4_DDCSCL_5V	18	5V_DDCSCL	PS_ON	23
24 IN	SLP_S4*	36	SLP_S5	RSMRST	42
24 IN	SLP_S3*	22	SLP_S3	YLW_LED	39
24 IN	GPIO_GRN_BLNK	37	GRN_BLNK	GRN_LED	40
24 IN	GPIO_YLW_BLNK	38	YLW_BLNK	HSYNC_5V	51
TP_GLUE4_HSYNC3V		49	HSYNC_3V	VSYNC_5V	52
TP_GLUE4_VSYNC3V		50	VSYNC_3V	STRAP	54
52 IN	GLUE4_5_PU	5	A20M/GP1_INB	GP3_OUT	56
25 23 OUT	V_REF5V_SUS	48	REF5V_STBY	GND	11
	VCCP_VREF	53	VCCP_VREF	GND	29
		55	GP3_IN	GND	43

GLUE4_VREF5IN_R		
GLUE4_VREF3IN_R		
V_5P0_STBY	IN	60 69
V_3P3_STBY	IN	63 69
V_REF5V	OUT	23 25
HD_LED*	OUT	55 74
P_RST_SLOTS_R*	OUT	52
TP_AUD_RST*		
TP_MUTE_AUD_PN1*		
TP_SCK_BJT_GATE_ENABLE		
TP_GLUE4_FLUSH_OUT_FWH		
TP_GLUE4_GP1_OUT		
TP_GLUE4_8		
IDE_RST*	OUT	27
BACKFEED_CUT	OUT	51 76
BACKFEED_CUT_LATCHED	OUT	51
PWRGD_3V	OUT	69 12 24 30 51 62
PS_ON*	OUT	60
RSMRST*	OUT	52
GPIO_YLW_BLNK_HDR	OUT	55 74
GPIO_GRN_BLNK_HDR	OUT	55 74
TP_GLUE4_HSYNC5V		
TP_GLUE4_VSYNC5V		
GLUE4_STRAP		
PWRGD_PS_BUFF	OUT	35

RP1J1 1K 5% .063W IC SM
RP2J1 10K 5% .063W IC SM

69 63 IN V_3P3_STBY — R2H8 100 603 1% CH — R2J1 49.9 1% CH 603
PWRGD_PS HAS WEAK INTERNAL PULL-UP

GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I

[PAGE_TITLE=GLUE4]

DRAWING
FAB_A.SCH.1.52
Mon Nov 18 12:30:26 2002
D845GFT FAB A

DOCUMENT NUMBER	PAGE	REV
C23021	52	4.0

CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP

Q1G2
MMBT3904
EMPTY
2 108969-001

603259-050
C1G2
1000PF
10%
50V
EMPTY
603

R2F6
0 1A
603 EMPTY

57 OUT CPU_FAN_PWM1
76 35 33 32 31 24 BI SMB_DATA_MAIN
76 35 33 32 31 24 BI SMB_CLK_MAIN
8 69 OUT H_TEMP_RET
69 8 IN H_TEMP_SRC
SE_ZONE_TDP
SE_ZONE_TDN
74 68 IN H_VID<4..0>

PRELIMINARY
U1F1
HECETA6

24	PWM1/NTESTOUT	VCCP_IN	23
		2.5V	22
1	SDA	5V	20
2	SCL	3.3SBY	4
		12V	21
18	REMOTE1+		
17	REMOTE1-/NTESTIN	PWM2	10
16	REMOTE2+	PWM3	13
15	REMOTE2-		
		TACH1	11
4 19	VID4	TACH2	12
3 8	VID3	TACH3	9
2 7	VID2	TACH4	14
1 6	VID1		
0 5	VID0	GND	3

EMPTY

VCCP IN 67 69
V_1P5_CORE IN 66
V_3P3_STBY IN 63 69
TP_HECETA6_PWM2_P10
FNT_REAR_FAN_PWM3 OUT 46 57
CPU_FAN_TACH IN 57
H6_TAC4_PD
FRONT_FAN_TACH IN 57
REAR_FAN_TACH IN 57

VCC
+12V
R1F7 0 1A EMPTY 603
R1F2 10K 5% EMPTY 603

ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4

NOTE
FOR PHILLIPS H4 SMBUS ADDR ISSUE

69 63 IN V_3P3_STBY
R1F3 1K 5% EMPTY 603
H4_RSTN_H6_PWM1
H4_VCC3_H6_12V

52 24 74 55 OUT FP_RST*
R2F4 0 1A 603 CH

U1F2
HECETA4

16	A0/NTEST_OUT	+VCCP_IN	15
		+2.5VIN	14
1	SDA	+5VIN	12
2	SCL	VDD/3.3VIN	4
		+3.3V	13
10	RMT_DIODE+		
9	RMT_DIODE-		
4 11	+12V/VID4		
3 8	VID3		
2 7	VID2	GNDD	3
1 6	VID1		
0 5	VID0		

IC

VCC3
R1F9 0 1A CH 603

C1F1 1UF 20% Y5V 603
C1F2 1UF 10% 16V X7R 603

ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6

SMBUS ADDRESS?

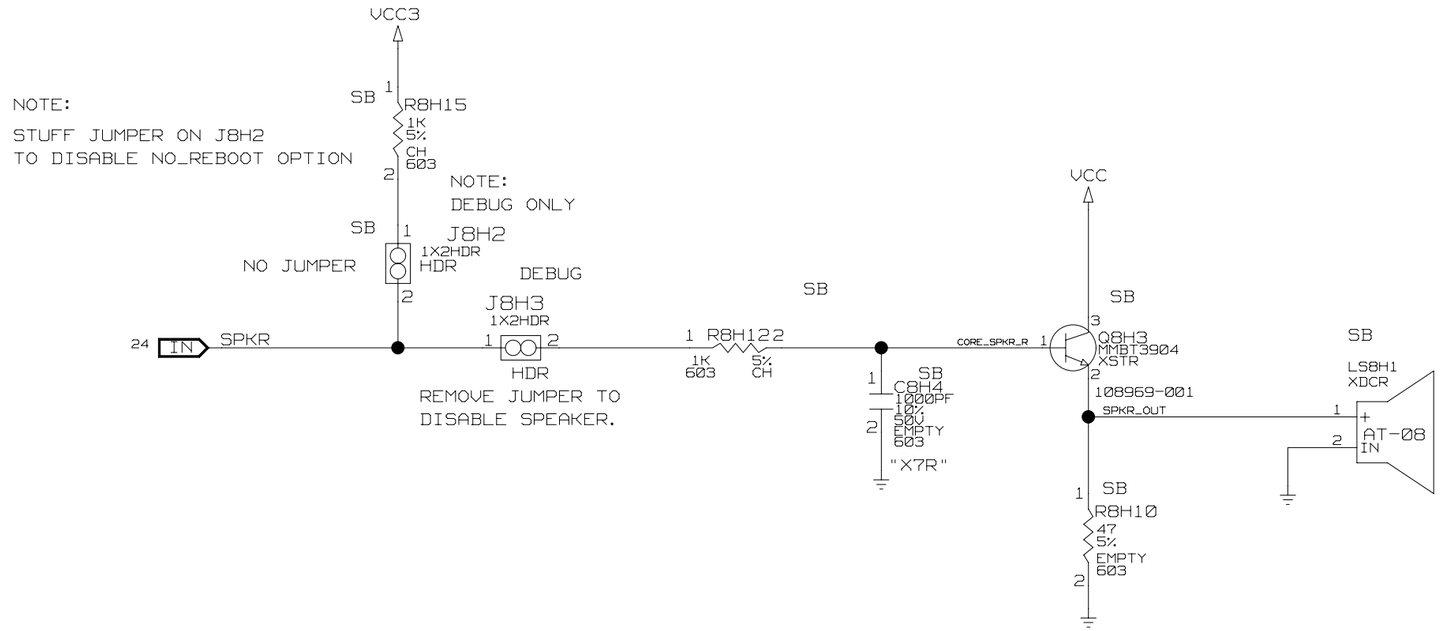
HARDWARE MANAGEMENT: HECETA†

[PAGE_TITLE=HECETA]

ROOM=HWM_HECETA4
BOM=HWM_HECETA4

DRAWING
FAB_A.SCH.1.53
Mon Nov 18 13:51:27 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	53	4.0



[PAGE_TITLE=SPEAKER]

DRAWING

FAB_A.SCH.1.54
Mon Nov 18 13:51:37 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	54	4.0

[FULL_ID=1164-59-16[illegible] [PAGE_INFO_ID=16505] [MODULE_ID=128-58-14[illegible] [DONOR_ID=1130-56-152381]

J9G2
2X3HDR_2
TP_IR_FP_1
VCC
55 46 OUT SIO_IRTX2
SIO_IRRX2 IN 55
HDR
109717-731

CAD NOTE: OVERLAY SO PINS
1-9 MATCH UP (DUAL FP).
J9G2 DOES NOT NEED TO BE DUAL FP'D

VCC
R9H8
0 603
1A EMPTY
FP_PWR_5V
STUFF R9H8 ONLY WHEN
J9H3 IS STUFFED

J9H2
2X5HDR_10
HDR
109717-010

V_5P0_STBY IN 60 69
R9H1 220 5% CH 603
R9H3 220 5% CH 603
GPIO_GRN_BLNK_HDR IN 52
GPIO_YLW_BLNK_HDR IN 52

R9H4
VCC3
10K 603 5% CH
R9H12
UNSTUFF FOR C
VCC
330 603 5% CH

52 IN HD_LED*
52 24 74 53 OUT FP_RST*
55 46 OUT SIO_IRRX2
55 46 IN SIO_IRTX2

J9H3
2X3HDR_4
VCC
EMPTY
109717-021

VCC
CP9H2 470PF 20% 50V EMPTY SM
CP9H2 470PF 20% 50V EMPTY SM
CP9H1 470PF 20% 50V EMPTY SM
602431-005 C9H2 470PF 10% 50V EMPTY 603
CP9H1 470PF 20% 50V EMPTY SM
"X7R"
CP9H1 470PF 20% 50V EMPTY SM
CP9H1 470PF 20% 50V EMPTY SM
CP9H2 470PF 20% 50V EMPTY SM
CP9H2 470PF 20% 50V EMPTY SM

BOM=CORE_STDFNTPNL_E

J9H1
1X3HDR2
102276-304
HDR
GPIO_GRN_BLNK_HDR IN 52
C9G5 470PF 10% 50V EMPTY 603
GPIO_YLW_BLNK_HDR IN 52
C9H1 470PF 10% 50V EMPTY 603

DECOUPLING
VCC3
C9G8 1UF 20% 50V Y5V 603
BOM = VREG_DCPL_BULK

69 63 IN V_3P3_STBY R9H6 22K 603 5% CH 202285-081
SW_ON* OUT 24
74 IN SWITCH_ON*
R9H102 33 603 5% CH
C9H4 1.0UF 10% 16V Y5V 603
202285-013

[PAGE_TITLE=STD_FRONT_PANEL_HDR]

DRAWING
FAB_A.SCH.1.55
Mon Nov 18 13:51:46 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	55	4.0

[DONOR_REV=1.02/page56] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page55] [PROJ_NAME= _G_DDR--1164] [MODULE=SIO] [SOLUTION=SMSC/LPC47B27X] [MOD_PAGE=PAGE 11] [MOD_REV=REV0_91C] [LAST_MAKEGOLD: 6/28/99 11:04:37am] [LAST_MAKEPROJ: 10/12/2001 1:57:05 PM]

MH8A1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH7A1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH1B1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH9G1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH7G1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH1G1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH7J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MH1J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

CONNECTOR LOCATION

	X	Y
PS/2	8525	6210
USB/LAN	7965	5927
COM	6940	6115
PAR	5362	5843
VGA	5136	6190
DIAGLED	4636	6045
USB	4151	6026
AUD	3291	6218

LABELS

DEBUG
LB5J1
LABEL
SILK
'KOREAN CERT' SILKSCREEN COVERED UNTIL CERTIFIED
MAKE EMPTY ON BOM

LBL
LB3J1
LABEL
A19177-001
1375X250_TARGET
MAKE ISN ON BOM

DEBUG
LB3F1
1 SILK
INTELtm
'INTEL' LOGO SILKSCREEN
2.0 X 0.250
MAKE EMPTY ON BOM

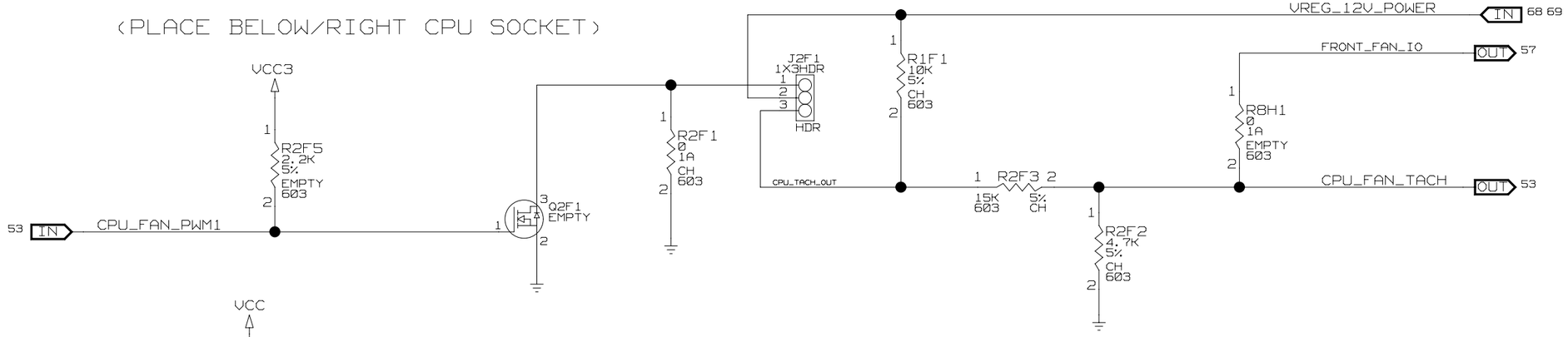
[PAGE_TITLE=LABELS_MOUNTING_HOLES]

DRAWING
FAB_A.SCH.1.56
Mon Nov 18 13:51:54 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	56	4.0

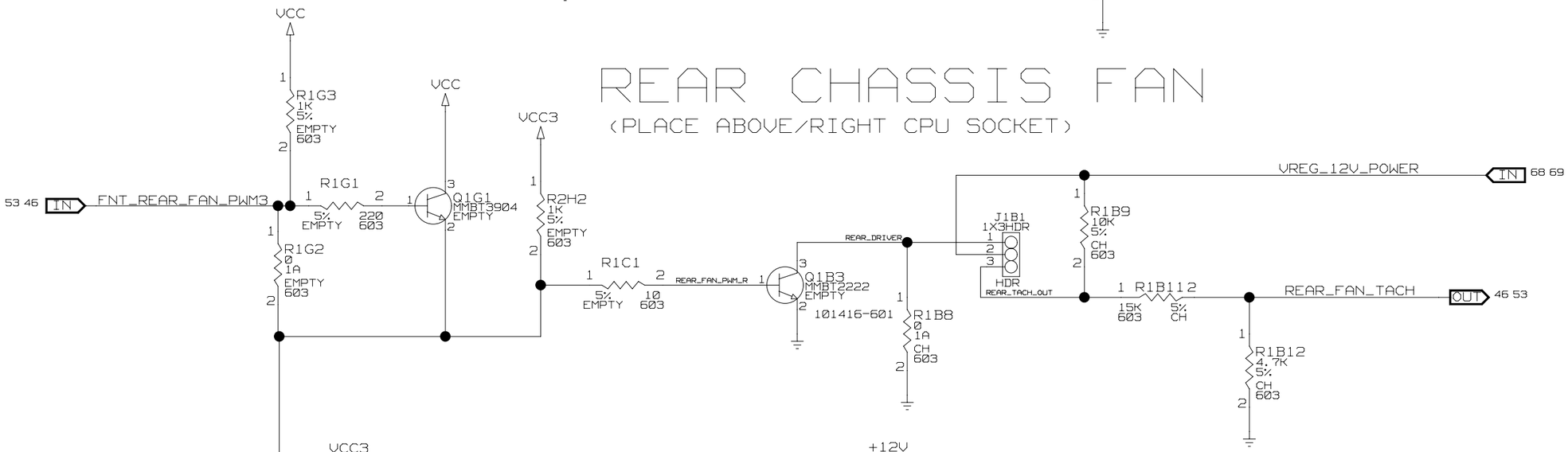
CPU ALWAYS-ON FAN

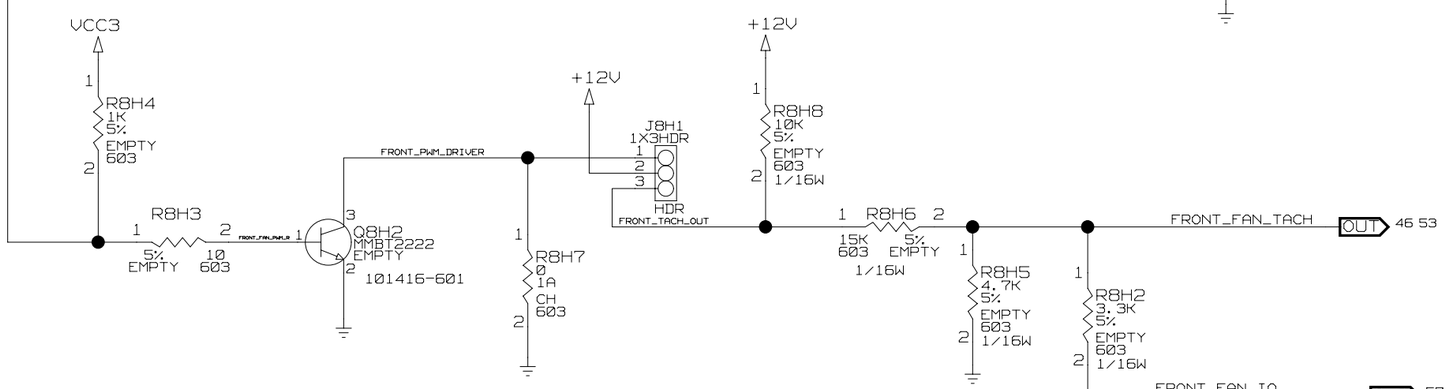
(PLACE BELOW/RIGHT CPU SOCKET)



REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)





FRONT CHASSIS FAN

(PLACE LOWER LEFT CORNER OF PLATFORM)

[PAGE_TITLE=FAN_CONTROL]

DRAWING

FAB_A.SCH.1.57
Mon Nov 18 13:52:04 2002
D845GFT FAB_A

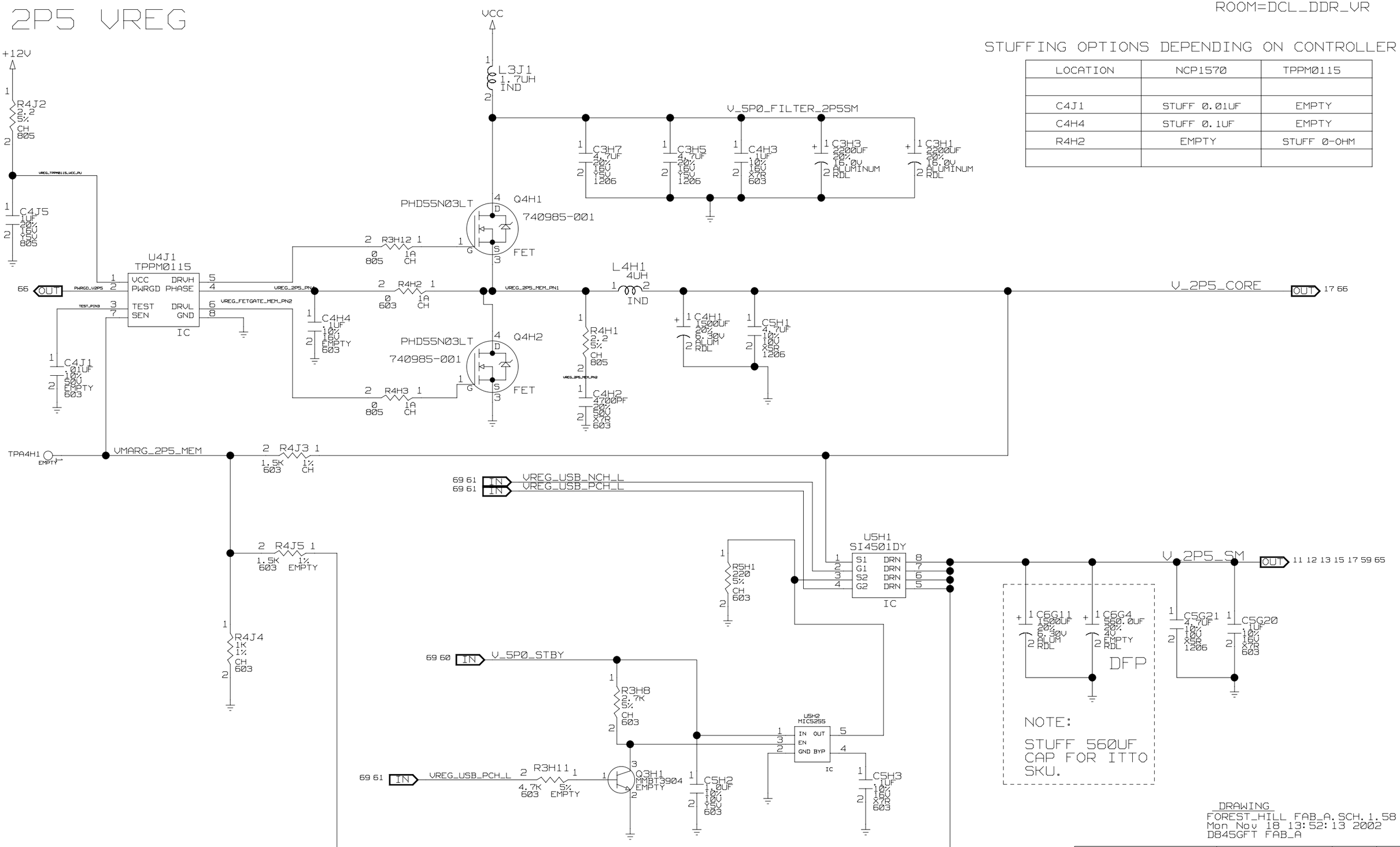
DOCUMENT NUMBER	PAGE	REV
C23021	57	4.0

2P5 VREG

ROOM=DCL_DDR_VR

STUFFING OPTIONS DEPENDING ON CONTROLLER

LOCATION	NCP1570	TPPM0115
C4J1	STUFF 0.01UF	EMPTY
C4H4	STUFF 0.1UF	EMPTY
R4H2	EMPTY	STUFF 0-OHM



DRAWING
FOREST_HILL FAB_A.SCH.1.58
Mon Nov 18 13:52:13 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	58	4.0

ROOM=DCL_DDR_VR

1.25V DDR

58 IN

V_2P5_SM

+12V

1 R3H5 10 5% CH 603 2

1 C3H4 1UF 10% 16V X7R 603 2

INV_A_PIN8

U2H1 LM358 IC

INV_A_OUT

INV_A_PIN4

2 R2H1 1 10 603 5% CH

+12V

2 C2H1 1UF 10% 16V X7R 603 1

BAT54C SOT23C DIO

CR2H1

3 Q3G1 FET D S G 1 2

1 R2G3 2 1K 603 5% CH

1 R3H1 49.9 1% CH 603 2

TPA3H1 EMPTY

INV_A_VTT

1 R3H3 2 0 603 1A CH

1 R3H2 49.9 1% CH 603 2

1 C3H2 1.0UF 10% 10V X5R 603 2

1 R2H3 0 1A EMPTY 603 2

V_1P25_MEMVTT

OUT 18 19 20

1 C2G18 470UF 20% 10V ALUM RDL 2

1 C5G19 470UF 20% 10V ALUM RDL 2

1 C3G3 4.7UF 10% 10V X5R 1206 2

1 C2G4 1UF 10% 16V X7R 603 2

2 Q2G1 MOSFET S D G 1 3

A61801-001

C2G19 470UF 20% 10V ALUM RDL

C3G16 470UF 20% 10V ALUM RDL

U2H1 LM358 IC

DIMM_VREF_1P25_R

R3H4 2 0 603 1A EMPTY

DIMM_VREF_1P25

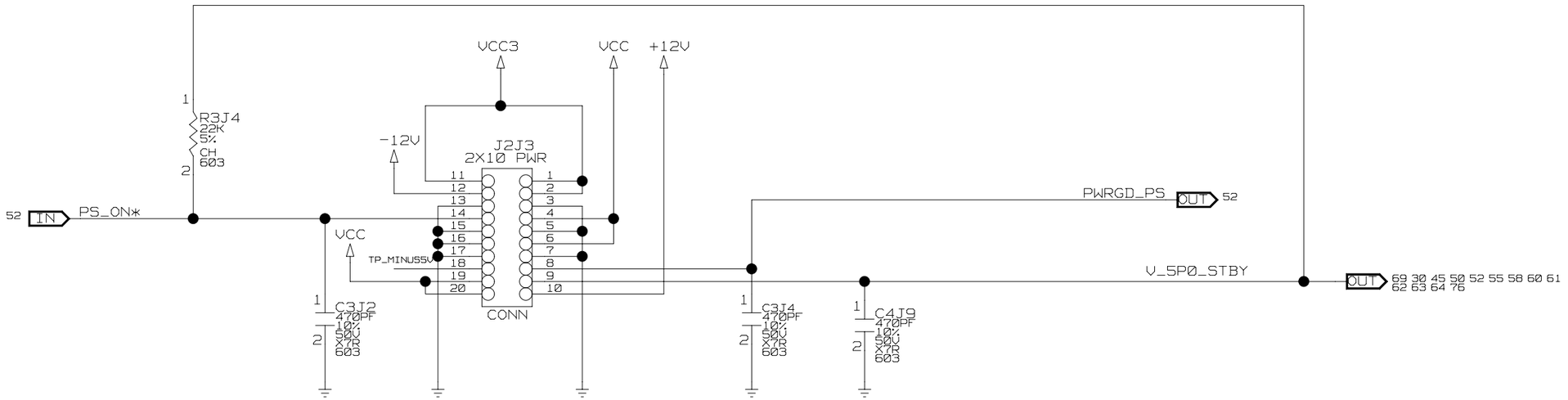
OUT 17 11 17

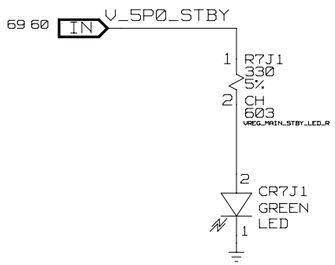
[PAGE_TITLE=2P5_VREG]

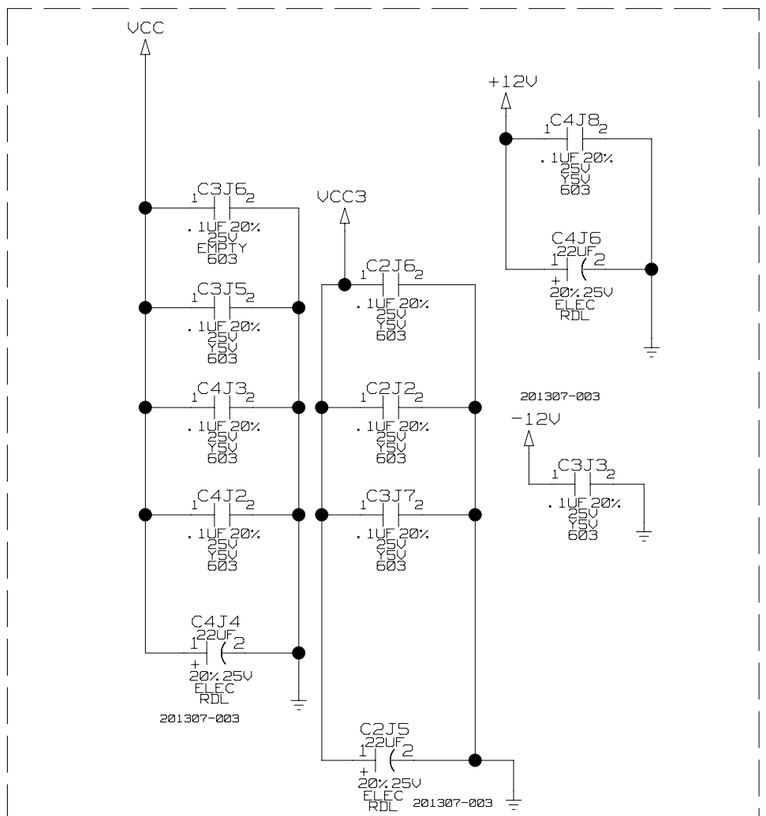
DRAWING

FAB_A.SCH.1.59
Mon Nov 18 13:52:21 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	59	4.0







STANDARD POWER CONNECTOR

DRAWING
FAB_A.SCH.1.60
Mon Nov 18 13:52:30 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	60	4.0

69 63 IN V_3P3_STBY

CR8G1 PWR

BAT54C SOT23C DIO

V_3P0_BAT_VREG OUT 24 25

PWR R8G13 1K 603 5% CH

VREG_VBAT_R

PWR BT8F1 2PCOIN

PWR C8G5 1.0UF 10% 10V X5V 603

CAD NOTE: PLACE NEAR ICH

V_BAT_VREG_R_CR OUT 25

THROUGH-HOLE

CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

USB/PS2 WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF

69 60 IN V_5P0_STBY

+12V

RP8C4 2.7K 5% .063W IC SM

RP8C4 2.7K 5% .063W IC SM

A R9F2 0 1A CH 603

B R8C5 0 1A CH 603

VREG_USB_PCH BI 61 30 62

VREG_USB_NCH BI 61 30 62

VREG_USB_NCH_L BI 69 58

VREG_USB_PCH_L BI 69 58

Q8C1 MBT3904DUAL

52 IN BACKFEED_CUT_LATCHED

RP8C4 2.7K 5% .063W IC SM

BFEED_CUT_LATCHED_RTN

XSTR

RP8C4 2.7K 5% .063W IC SM

62 30 61 BI VREG_USB_PCH

62 30 61 BI VREG_USB_NCH

C R8C6 0 1A EMPTY 603

D R9F1 0 1A EMPTY 603

69 60 IN V_5P0_STBY

+12V

R8C7 2.7K 5% CH 603

R9E1 2.7K 5% CH 603

VCC3

U8B2 SI4501DY

S1 S2 G1 G2 DRN DRN DRN DRN

IC A03106-001

BFEED_CUT_PU_12V

BFEED_CUT_PU_5STBY

69 63 IN V_3P3_STBY

Q8D1 MBT3904DUAL

52 IN BACKFEED_CUT

XSTR

NOTE:
GLUE4 HAS OD OUTPUT.
PULLUP ON GLUE4 PAGE PROVIDES BASE CURRENT.

C8C2 100UF 20% 25V FTLEC RDL

CAD NOTE: PLACE AT PCI SLOTS

C8C1 .1UF 20% 50V X5V 603

C9C3 .1UF 20% 50V X5V 603

C7C4 .1UF 20% 50V X5V 603

C9C2 .1UF 20% 50V X5V 603

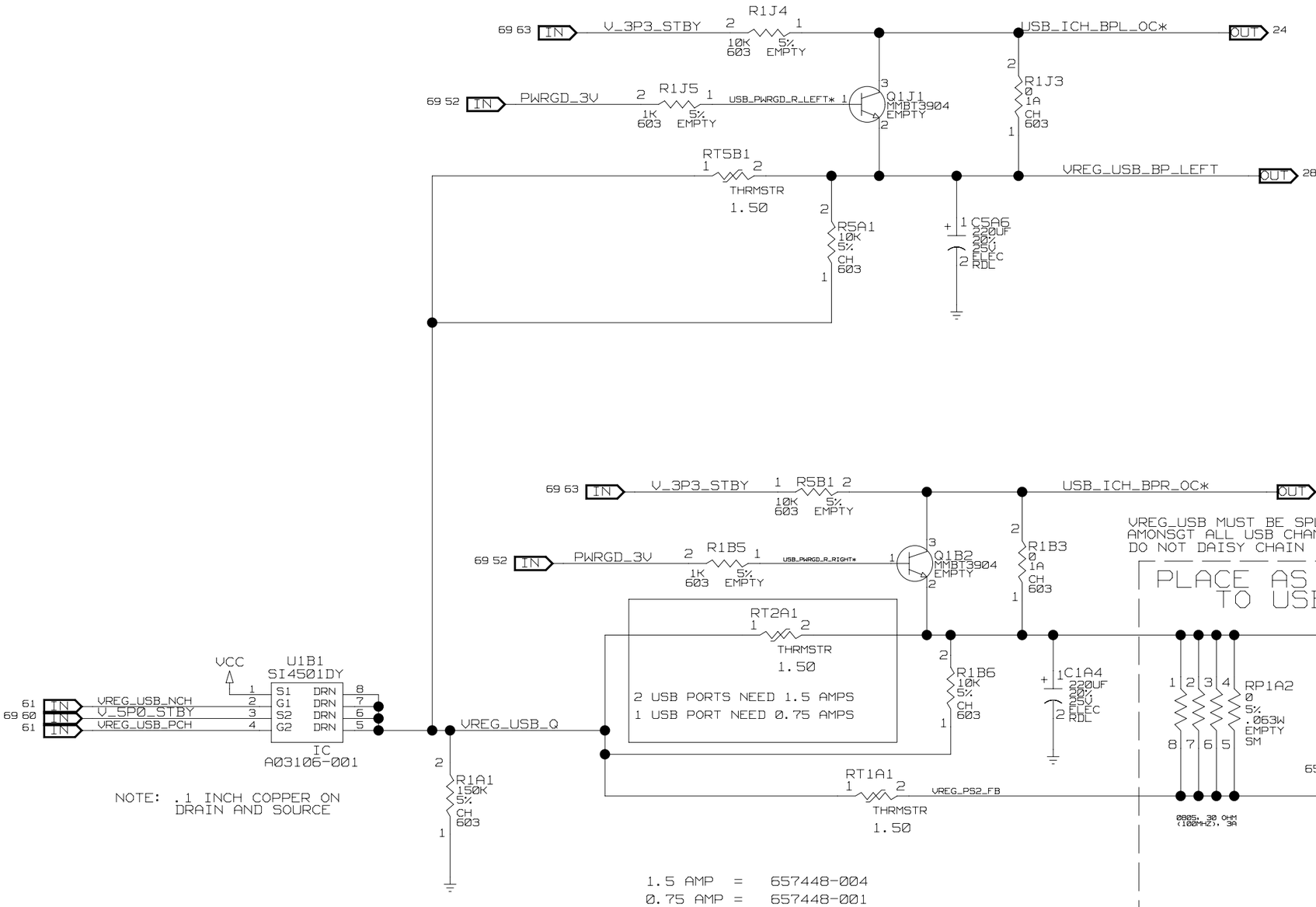
V_3P3_PCIVAUX OUT 69 72 21 31 32 33 36 74

PRODUCT BOARDS MAY EMPTY

PCI VAUX

DRAWING
FAB_A.SCH.1.61
Mon Nov 18 13:52:39 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	61	4.0

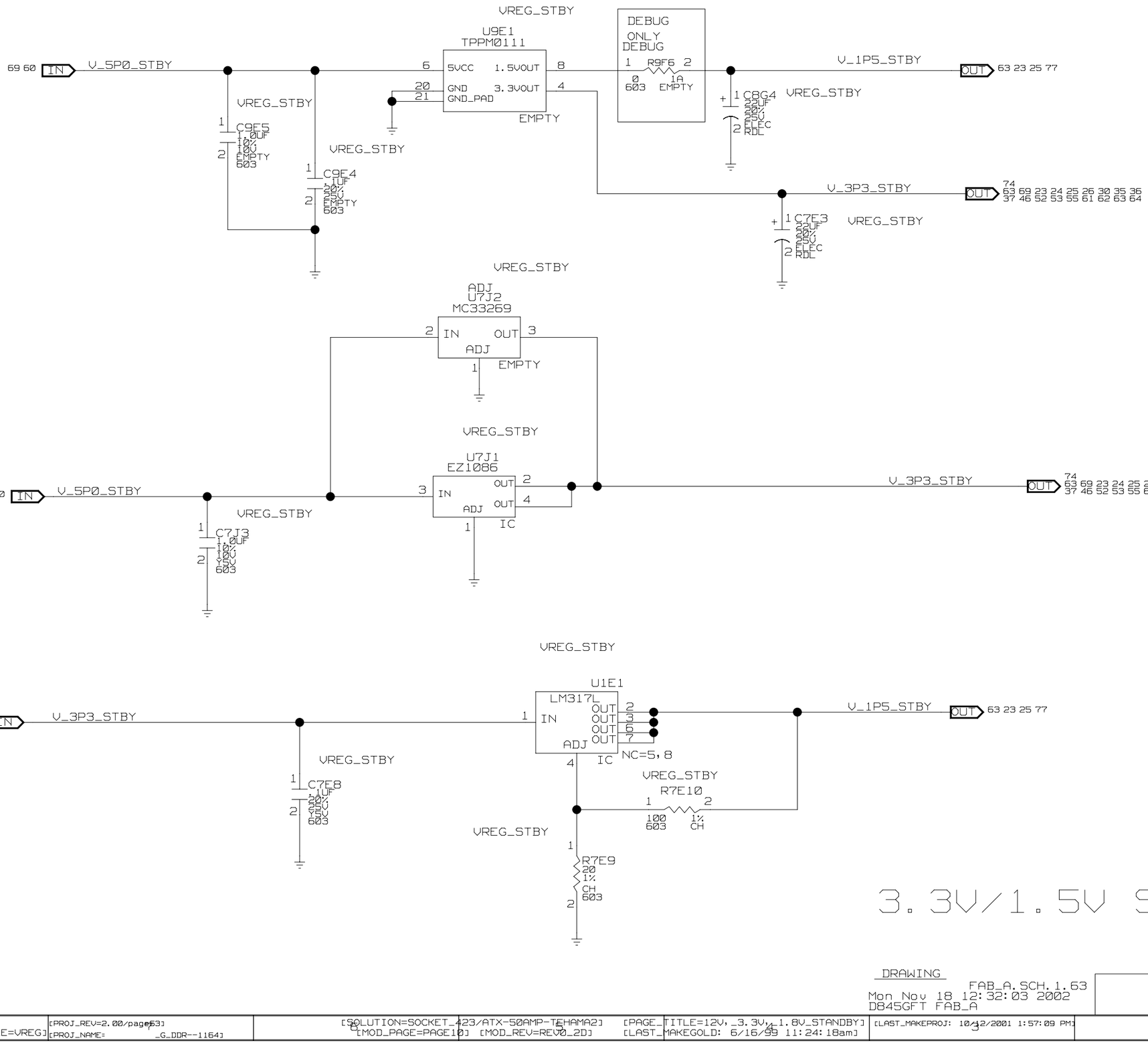


DRAWING

FAB_A.SCH.1.62
Mon Nov 18 13:52:48 2002
D845GFT FAB_A

WAKE ON USB & PS2

	DOCUMENT NUMBER	PAGE	REV
	C23021	62	4.0



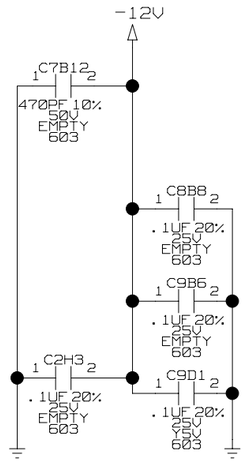
3.3V/1.5V STANDBY

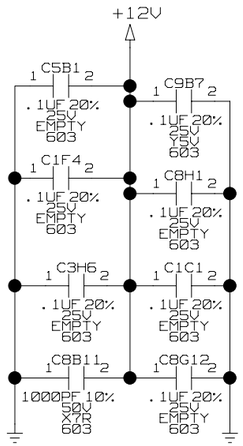
DRAWING

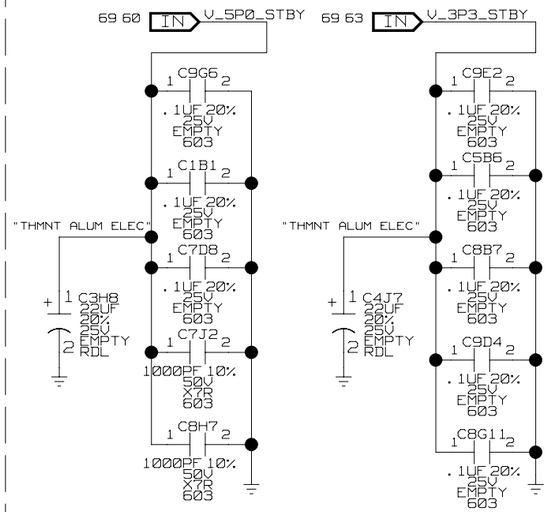
FAB_A.SCH.1.63
Mon Nov 18 12:32:03 2002
D845GFT FAB_A

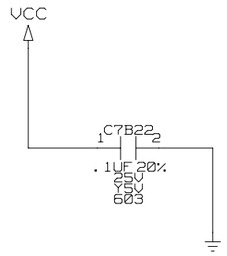
	DOCUMENT NUMBER	PAGE	REV
	C23021	63	4.0

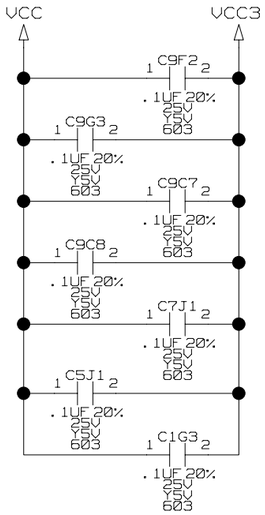
VREG_DCPL_BULK

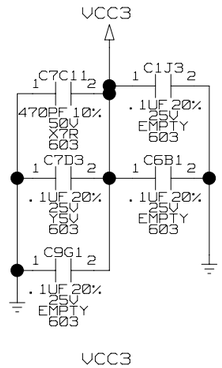


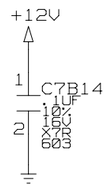


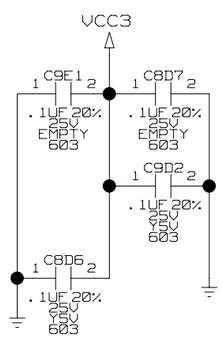


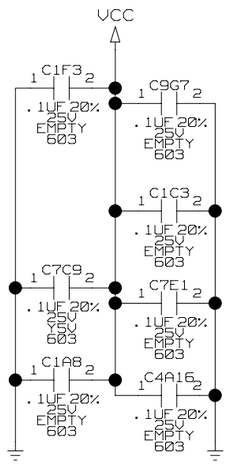


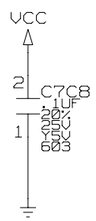


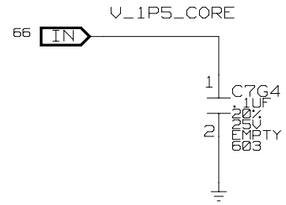


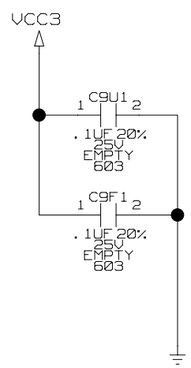


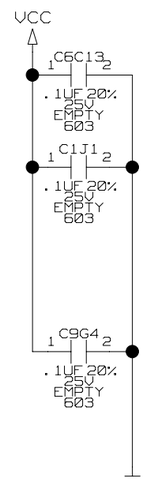


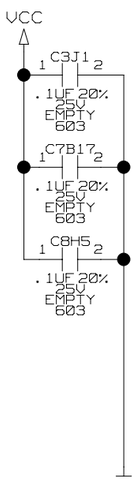


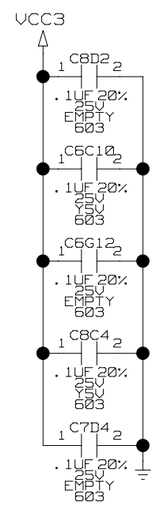












[PAGE_TITLE=VREG]

ROOM=DCPL_BULK
BOM=VREG_DCPL_BULK

DRAWING FAB_A.SCH.1.64
Mon Nov 18 13:52:58 2002
D845GFT FAB_A

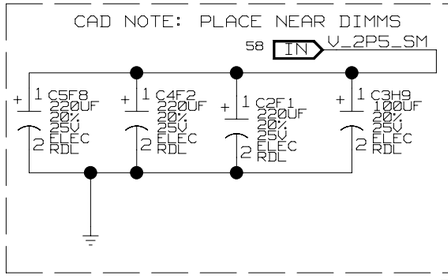
DOCUMENT NUMBER	PAGE	REV
C23021	64	4.0

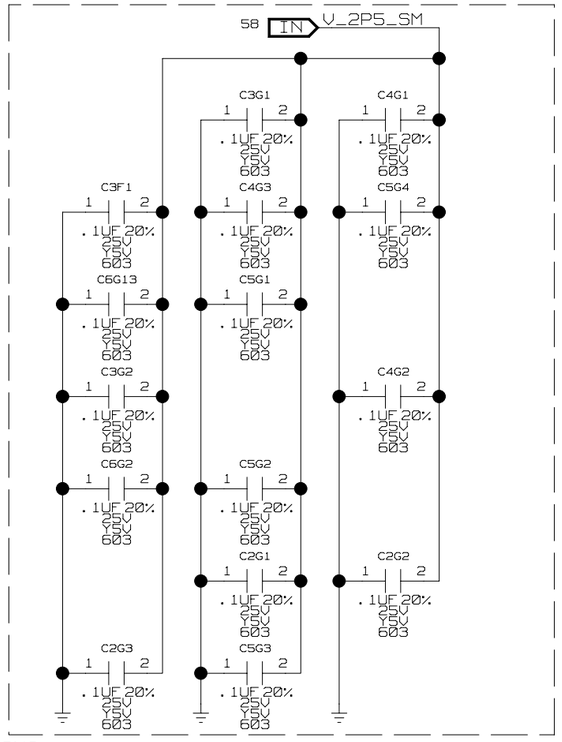
[FULL_ID=1164-71-165301] [PAGE_INFO_ID=16530] [MODULE_ID=1130-68-15262] [DONOR_ID=1130-68-15262]
[DONOR_REV=1.02/page66] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page64] [PROJ_NAME= _G_DDR--1164] [MODULE=VREG] [SOLUTION=SOCKET_423\ATX-50AMP-TEHAMA21] [MOD_PAGE=page63] [LAST_MAKEPROJ: 10/12/2001 1:57:10 PM] [MOD_REV=wtvv_pdt/0.07]

ROOM=DCL_DDR_DCPL

DDR 2P5_SM DECOUPLING

CAD NOTE: PLACE NEAR DIMMS



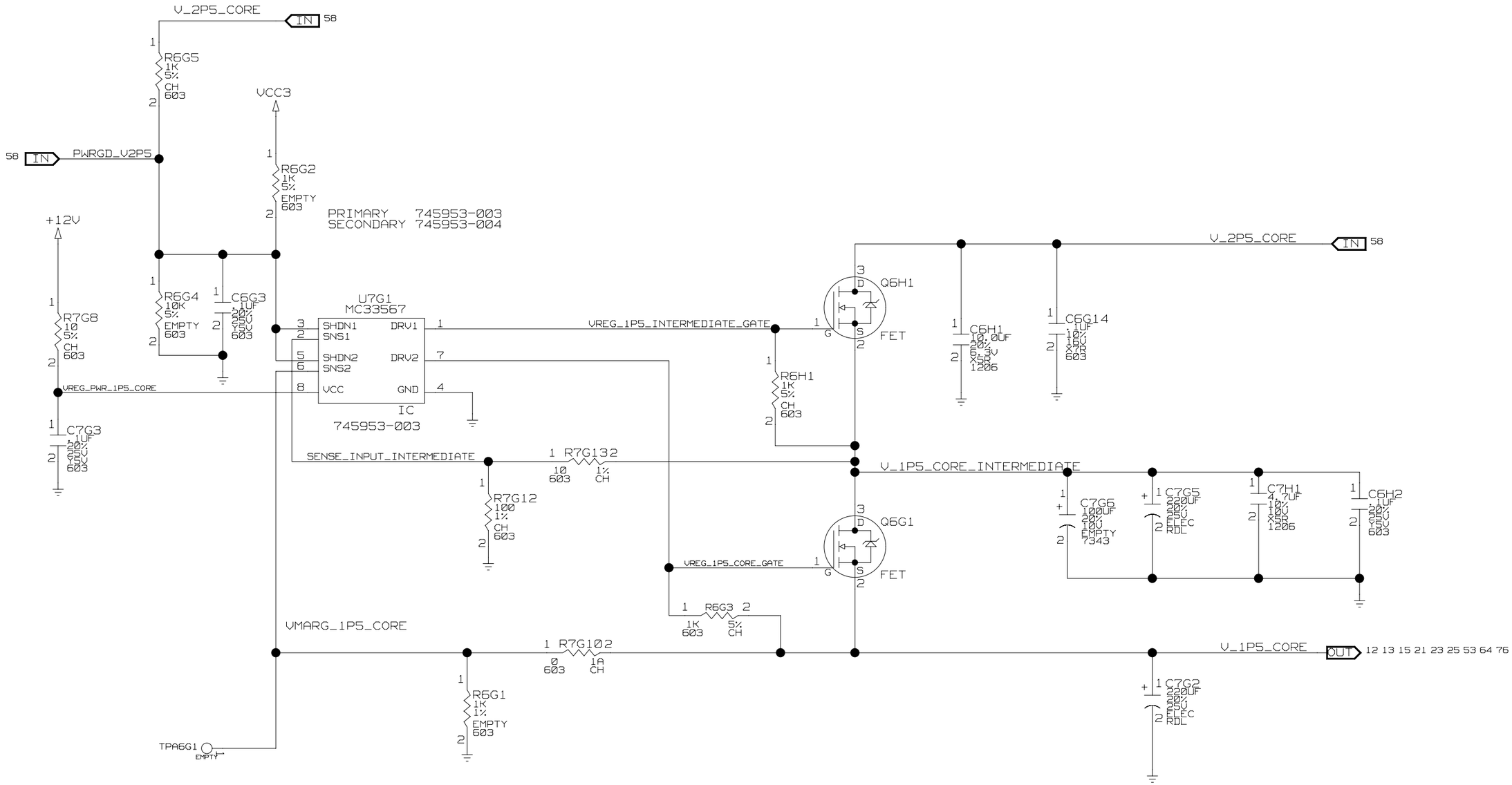


DRAWING

FAB_A.SCH.1.65
Mon Nov 18 13:53:07 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	65	4.0

[FULL_ID=1164-74-16536] [PAGE_INFO_ID=16536] [MODULE_ID=1130-71-15268] [DONOR_ID=1130-71-15268]



[PAGE_TITLE=1.5_VREG]

DRAWING
FAB_A.SCH.1.66
Mon Nov 18 13:53:17 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	66	4.0

[DONOR_REV=1.02/page 71] [MODULE=VREG] [PROJ_REV=2.00/page 66]
[DONOR_PROJ=NBVV_DDR--1130] [PROJ_NAME= _G_DDR 2.0A] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_REV=REV0_2D] [MOD_PAGE=PAGE12] [LAST_MAKEPROJ: 10/12/2001 1:57:11 PM] [LAST_MAKEGOLD: 6/16/99 11:24:26am]

[FULL_ID=1164-75-16538] [PAGE_INFO_ID=16538] [OWNED_BY=DE] [MODULE_ID=1164-75-16538] [DONOR_ID=1164-75-16538]

COMPOMENTS ARE DFM 29

VCC
R1B1 10K 603 5% CH
PWRGD_CNTR
MBT3904DUAL
Q1B1
9 IN VCC_VIDGD
XSTR

+12V
R1C2 2.4K 603 5% CH
Q1C1 PZT2222A XSTR
CR1C1 DIO 0.225W 5.8V
C1B6 4.7UF 20% 16V X5R 1206
REG_VCC_CS5323
CAD: PLACE CLOSE TO PZT2222
C1B5 4.7UF 20% 16V X5R 1206
R1B7 0 1A EMPTY 805

C1B2 .022UF 10% 50V X7R 603
AGND_A OUT 67
ANALOG GROUND

C2B4 .1UF 10% 50V X7R 603
R2B1 20 1% CH 603
C2B2 0.068UF 10% 50V X7R 603
R2B2 5.76K 603 1% CH
R2B3 1K 5% EMPTY 603
R2B4 1.15K 1% CH 603
C2B3 .22UF 10% 16V X7R 805
R2B5 15K 1% CH 603
R2B6 1.2K 603 5% CH
RT2B1 THRMSTR
FROM SOCKET BY ETCH GND RESISTOR
VCCP IN 67 69

R2B2 56.2K 603 1% CH
AGND_A OUT 67
ANALOG GROUND

U2B1 CS5323
OSC_A 1 ROSC
COMP_A2 COMP
VFB_A 3 VFB
VDRP_A4 VDRP
ILIM_A9 ILIM
10 REF
VID4 15
VID3 14
VID2 13
VID1 12
VID0 11
VCC 20 REG_VCC
GATE3 17 GATE3_A
GATE2 18 GATE2_A
GATE1 19 GATE1_A
CSREF 8 CSREF_A
CS1 5
CS2 6
CS3 7
GND 16
IC

H_VID<4..0> 74 68 IN

R1B4 2.2 5% CH 805
C1B4 4.7UF 20% 16V X5R 1206
C1B3 1.0UF 10% 16V X5R 805
AGND
OUT 67
ANALOG GROUND

VREG_12V_POWER IN 68 69
R4B3 0 805 1A CH
C4B3 .22UF 20% 16V Y5V 805
R4B2 2.2 5% CH 805
R4B4 2.2 5% EMPTY 805
C4B1 4700PF 20% 50V X7R 603
C4B2 1.0UF 10% 16V X5R 805
U4B1 HIP6601
VCC BOOT
GND UGATE
PWM PHASE
PVCC LGATE
VREGA_PWM2_G_DRV_H
VREGA_PWM2_G_DRV_L
IC

C2B8 .022UF 10% 50V X7R 603
R2B9 4.7K 603 5% CH
C2B7 .022UF 10% 50V X7R 603
C2B6 .022UF 10% 50V X7R 603
C2B5 .022UF 10% 50V X7R 603
VREGA_PWM3_SENSE_R
VREGA_PWM2_SENSE_R
VREGA_PWM1_SENSE_R
REF_A
R2B10 1K 5% CH 603
C2B9 1UF 10% 16V X7R 603
R1B10 1.5K 5% CH 603
JDR2P1 00HM EMPTY SM
FROM SOCKET
AGND_A
IN 67 ANALOG GROUND
R2B8 15K 1% CH 603
R2B7 15K 1% CH 603
VREGA_PWM1_SENSE IN 67
VREGA_PWM2_SENSE IN 67
VREGA_PWM3_SENSE IN 67

VCCP IN 67 69
FROM NEAREST INDUCTOR
VREG_12V_POWER IN 68 69
R3B3 0 805 1A CH
C3B3 .22UF 20% 16V Y5V 805
R3B2 2.2 5% CH 805
R3B4 2.2 5% EMPTY 805
C3B1 4700PF 20% 50V X7R 603
C3B2 1.0UF 10% 16V X5R 805
U3B1 HIP6601
VREGA_PWM1_G_DRV_H
VREGA_PWM1_G_DRV_L
IC

R5B4 2.2 5% EMPTY 805
C5B12 4700PF 20% 50V X7R 603
R5C3 2.2 5% CH 805
C5B11 4700PF 20% 50V X7R 603
C5B9 1.0UF 10% 16V X5R 805
U5B1 HIP6601
VREGA_PWM3_G_DRV_H
VREGA_PWM3_G_DRV_L
IC

68 IN VREG_12V_FILTERED
C5B8 4.7UF 20% 16V Y5V 1206
Q5B1 A55421-001 FET
Q4C2 Q4C1 Q4B5 FET
A65852-001
VREGA_PWM3_SENSE OUT 67
L4B1 450NH IND

68 IN VREG_12V_FILTERED
C3A13 4.7UF 20% 16V Y5V 1206
Q4B1 A55421-001 FET
Q4B2 Q4B3 Q4B4 FET
A65852-001
VREGA_PWM2_SENSE OUT 67
L3B1 450NH IND
VCCP OUT 25 53 67 68 69 7 8 10 12 15 23 71 76

68 IN VREG_12V_FILTERED
C2A9 4.7UF 20% 16V Y5V 1206
Q2B1 A55421-001 FET
Q3B1 Q3B2 Q3B3 FET
A65852-001
L2B1 450NH IND
VREGA_PWM1_SENSE OUT 67

[PAGE_TITLE=DECOUPLING]

DRAWING
FAB_A.SCH. 1.67
Mon Nov 18 13:53:27 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	67	4.0

[FULL_ID=1164-76-16540] [PAGE_INFO_ID=16540] [OWNED_BY=DE] [MODULE_ID=1130-73-15272] [DONOR_ID=1130-73-15272]

ROOM = DCL_CORE_CPU_VREG

69 67 IN VCCP

C3C2 10.0UF 20% 4V X5R 1206
C2C1 10.0UF 20% 4V X5R 1206
C3C4 10.0UF 20% 4V X5R 1206
C3C8 10.0UF 20% 4V X5R 1206
C2C4 10.0UF 20% 4V X5R 1206
C2C2 10.0UF 20% 4V X5R 1206
C3C3 10.0UF 20% 4V X5R 1206
C2C5 10.0UF 20% 4V X5R 1206
C2C7 10.0UF 20% 4V X5R 1206
C3C9 10.0UF 20% 4V X5R 1206
C2C8 10.0UF 20% 4V X5R 1206
C2C3 10.0UF 20% 4V X5R 1206
C2C6 10.0UF 20% 4V X5R 1206
C2C9 10.0UF 20% 4V X5R 1206

NOTE: PLACE THESE NORTH OF THE CPU SOCKET

C2D2 10.0UF 20% 4V X5R 0805
C2D1 10.0UF 20% 4V X5R 0805
C2D3 10.0UF 20% 4V X5R 0805
C2D8 10.0UF 20% 4V X5R 0805
C2D9 10.0UF 20% 4V X5R 0805
C2D4 10.0UF 20% 4V X5R 0805
C2D10 10.0UF 20% 4V X5R 0805
C2D7 10.0UF 20% 4V X5R 0805
C2D13 10.0UF 20% 4V X5R 0805
C2D11 10.0UF 20% 4V X5R 0805
C2D6 10.0UF 20% 4V X5R 0805
C2D14 10.0UF 20% 4V X5R 0805
C2D15 10.0UF 20% 4V X5R 0805
C2D12 10.0UF 20% 4V X5R 0805
C2D18 10.0UF 20% 4V X5R 0805
C2D5 10.0UF 20% 4V X5R 0805
C2D17 10.0UF 20% 4V X5R 0805
C2D16 10.0UF 20% 4V X5R 0805

NOTE: PLACE THESE IN THE CAVITY OF THE CPU SOCKET

C3F2 10.0UF 20% 4V X5R 0805
C3F1 10.0UF 20% 4V X5R 0805
C2F4 10.0UF 20% 4V X5R 0805
C2F2 10.0UF 20% 4V X5R 0805
C2F1 10.0UF 20% 4V X5R 0805
C2F3 10.0UF 20% 4V X5R 0805

NOTE: PLACE THESE SOUTH OF THE CPU SOCKET

C2B11 560.0UF 20% 4V ALUM RDL
C2B13 560.0UF 20% 4V ALUM RDL
C2B10 560.0UF 20% 4V ALUM RDL
C3B5 560.0UF 20% 4V ALUM RDL
C4B5 560.0UF 20% 4V ALUM RDL
C4B4 560.0UF 20% 4V ALUM RDL
C4C1 560.0UF 20% 4V ALUM RDL
C4B6 560.0UF 20% 4V ALUM RDL
C2B12 560.0UF 20% 4V ALUM RDL

L5C1 PWR 1.7UH IND

C4C3 560.0UF 20% 2V EMPTY RDL
C3B6 3300UF 20% 2.5V ALUM RDL
DFP

C3B4 560.0UF 20% 2V EMPTY RDL
C4C4 3300UF 20% 2.5V ALUM RDL
DFP

C5C2 560.0UF 20% 2V EMPTY RDL
C5C3 3300UF 20% 2.5V ALUM RDL
DFP

VREG_12V_FILTERED

OUT 67

VREG_12V_POWER

OUT 69 57 67 74

C5B7 2200UF 20% 16.0V ALUMINUM RDL
C5B10 2200UF 20% 16.0V ALUMINUM RDL
C2B1 2200UF 20% 16.0V ALUMINUM RDL

A27641-001
J5C1
2X2HDR PWR
CONN

C5C4 470PF 10% 50V EMPTY 603 "Y5V"
C5C5 470PF 10% 50V EMPTY 603 "Y5V"

67 53 74 OUT H_VID<0> R1F152 1K 603 5% CH
67 53 74 OUT H_VID<1> R1F142 1K 603 5% CH
67 53 74 OUT H_VID<2> R1F132 1K 603 5% CH
67 53 74 OUT H_VID<3> R1F122 1K 603 5% CH
67 53 74 OUT H_VID<4> R1F112 1K 603 5% CH

VCC3

CAPACITORS

[PAGE_TITLE=CPU_VREG]

DRAWING
FAB_A.SCH.1.68
Mon Nov 18 12:32:53 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	68	4.0

[DONOR_REV=1.02/page73] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page68] [PROJ_NAME= _G_DDR--1164] [MODULE=NONE] [LAST_MAKEPROJ: 10/12/2001 1:57:13 PM]

ROOM=DCL_TRACK_SPLIT

76 24 11	BI	HI<0>
76 24 11	BI	HI<1>
76 24 11	BI	HI<2>
76 24 11	BI	HI<3>
76 24 11	BI	HI<4>
76 24 11	BI	HI<5>
76 24 11	BI	HI<6>
76 24 11	BI	HI<7>
76 24 11	BI	HI<8>
76 24 11	BI	HI<9>
76 24 11	BI	HI<10>
76 24 11	BI	HI_STBS
76 24 11	BI	HI_STBF
76 11 15	BI	HI_VREF_GMCH
76 8 77 24	BI	H_SMI*
8 77 24	BI	H_STPCLK*
8 53	BI	H_TEMP_RET
53 8	BI	H_TEMP_SRC
74 8	BI	H_VID_ISOLATE<4>
74 8	BI	H_VID_ISOLATE<3>
74 8	BI	H_VID_ISOLATE<2>
74 8	BI	H_VID_ISOLATE<1>
74 8	BI	H_VID_ISOLATE<0>
22 13	BI	VGA_RED
22 13	BI	VGA_RED*
22 13	BI	VGA_GREEN
22 13	BI	VGA_GREEN*

24 9	BI	H_THERMTRIP_ICH*
62 51 30 24 12 52	BI	PWRGD_3V
11 15	BI	HI_VSWING_GMCH
46 7	BI	CK_14M_SIO
24 7	BI	CK_14M_ICH
74 52 8	BI	H_SKTOCC*
58 61	BI	VREG_USB_PCH_L
58 61	BI	VREG_USB_NCH_L
52 71 8	BI	H_DBR*
75 74 52 51 46 11 25 76	BI	P_PCIRST*
69 36 35 17 7	BI	SMB_DATA_ISO
69 36 35 17 7	BI	SMB_CLK_ISO
8 24	BI	H_A20M*
8 24	BI	H_SLP*
24 9 8	BI	H_FERR*
8 24	BI	H_IGNNE*
51 8 24	BI	H_INIT*
8 24	BI	H_INTR
8 24	BI	H_NMI
8 24 9	BI	H_PWRGD
22 13	BI	VGA_BLUE
22 13	BI	VGA_BLUE*
24 7	BI	CK_48M_ICH_USB
76 24 7	BI	CK_66M_ICH
52 7	BI	CK_66M_GLUE
33 7	BI	CK_P_33M_S1
32 7	BI	CK_P_33M_S2

31 7	BI	CK_P_33M_S3
7	BI	CK_P_33M_S4
7	BI	CK_P_33M_S5
7	BI	CK_P_33M_S6
23 7	BI	CK_P_33M_ICH
51 7	BI	CK_P_33M_FWH
75 7	BI	CK_P_33M_PORT80
46 7	BI	CK_P_33M_SIO
38 7	BI	CK_14M_AUD
23 34 31 21	BI	P_INTA*
23 34 31 21	BI	P_INTB*
23 33 32 31 21	BI	P_PME*
33 32 31 52 21	BI	P_RST_SLOTS*
74 36 33 32 31 21 72 61	BI	V_3P3_PCIVAUX
52 13	BI	GLUE4_DDCSDA_3V
52 13	BI	GLUE4_DDCSCL_3V
22 13	BI	HSYNC_5V
22 13	BI	VSYNC_5V
		-12V
		+12V
		+12V
		+12V
		VCC3
74 64 36 35 30 26 25 24 23 63 63 62 61 55 53 52 46 37	BI	V_3P3_STBY
60 58 55 52 50 45 30 60 76 64 63 62 61	BI	V_5P0_STBY
23 15 12 10 9 8 7 67 76 71 68 67 53 25	BI	VCCP
74 67 57 68	BI	VREG_12V_POWER
69 36 35 17 7	BI	SMB_DATA_ISO
69 36 35 17 7	BI	SMB_CLK_ISO

TS01 TS02 TS03 TS04 TS05 TS06 TS07 TS08 TS09 TS10 TS11 TS12 TS13 TS14 TS15 TS16 TS17 TS18 TS19 TS20 TS21 TS22 TS23 TS24 TS25 TS26 TS27

TS28 TS29 TS30 TS31 TS32 TS33 TS34 TS35 TS36 TS37 TS38 TS39 TS40 TS41 TS42 TS43 TS44 TS45 TS46 TS47 TS48 TS49 TS50 TS51 TS52 TS53 TS54

TS55 TS56 TS57 TS58 TS59 TS60 TS61 TS62 TS63 TS64 TS65 TS66 TS67 TS68 TS69 TS70 TS71 TS72 TS73 TS74 TS75 TS76 TS77 TS78

TS80 TS81 TS83 TS84 TS86 TS87

[MODULE=CORES]

DRAWING
FAB_A.SCH.1.69
Mon Nov 18 13:56:16 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	69	4.0

[FULL_ID=1164-77-16542] [PAGE_INFO_ID=16542] [MODULE_ID=1130-74-15274] [DONOR_ID=1130-74-15274]

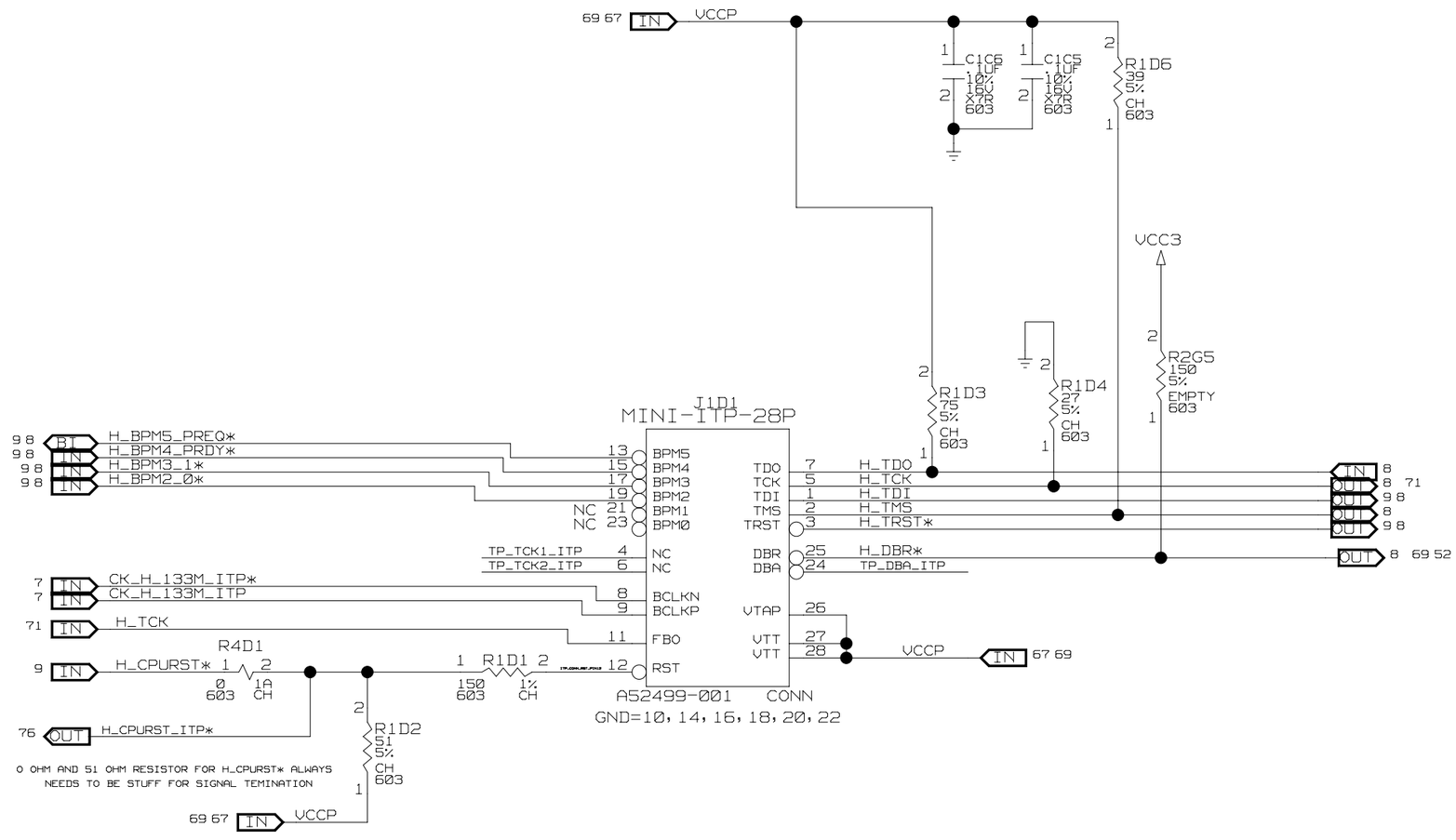
DEBUG PAGES

DRAWING
FAB_A.SCH.1.70
Mon Nov 18 12:47:56 2002
D845GFT FAB_A

	DOCUMENT NUMBER	PAGE	REV
	C23021	70	4.0

[DONOR_REV=1.02/page=74] [MODULE=VREG] [PROJ_REV=2.00/page=70] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [PAGE_TITLE=VREG_VCCP_CAP_DECOUPLING] [LAST_MAKEPROJ: 10/12/2001 1:57:13 PM]
[DONOR_PROJ=NBVV_DDR--1130] [PROJ_NAME= _G_DDR--1164] [MODULE=VREG] [MOD_PAGE=PAGE3] [MOD_REV=REV0_2D] [LAST_MAKEGOLD: 6/16/99 11:24:12am]

ITP 700FLEX CONNECTOR



CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.

SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

CAN THE ITP HANDLE A 5VSB PULLUP ON DBR

DRAWING FAB_A.SCH.1.71
Mon Nov 18 13:56:25 2002
D845GFT FAB_A

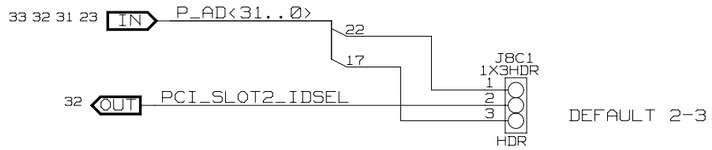
	DOCUMENT NUMBER	PAGE	REV
	C23021	71	4.0

[FULL_ID=1164-78-165441] [PAGE_INFO_ID=16544] [MODULE_ID=1130-75-15276] [DONOR_ID=1130-75-15276]

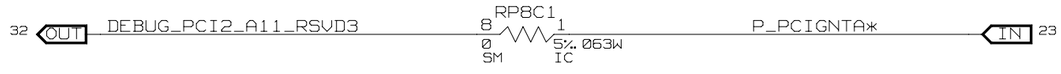
DEBUG HOOKS MOON ISA

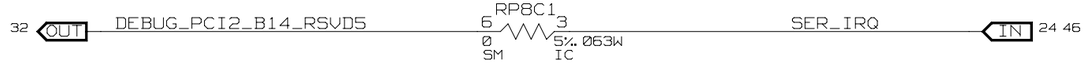
DEFAULT 2-3

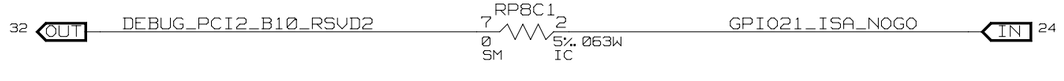
J8B3/J8C1	PCI SLOT 2 MODE
1-2	MOON ISA
2-3	PCI (DEFAULT)

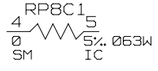


DEFAULT 2-3









[PAGE_TITLE=MOON_ISA]

DRAWING
FAB_A.SCH.1.72
Mon Nov 18 12:33:26 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	72	4.0

[DONOR_REV=1.02/page75] [DONOR_PROJ=NBVV_DDR--1130] [PROJ_REV=2.00/page72] [PROJ_NAME= G_DDR--1164] [MODULE=CORES] [SOLUTION=PERFORMANCE/WTVV] [MOD_PAGE=page61] [LAST_MAKEPROJ: 10/12/2001 1:57:14 PM] [MOD_REV=wtvv_pdt/0.07]

[FULL_ID=1164-79-1[illegible] [PAGE_INFO_ID=16546] [OWNED_BY=DE] [MODULE_ID=128-19-1[illegible] [DONOR_ID=1130-76-15278]

D C B A

INTETIONALLY LEFT BLANK

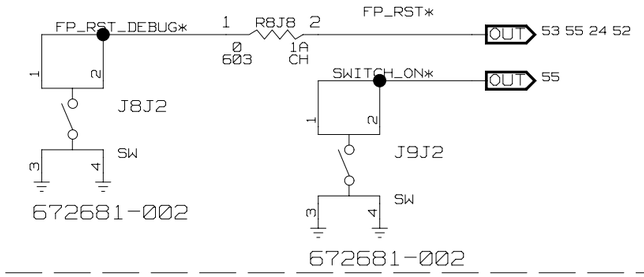
[PAGE_TITLE=BACKSIDE]

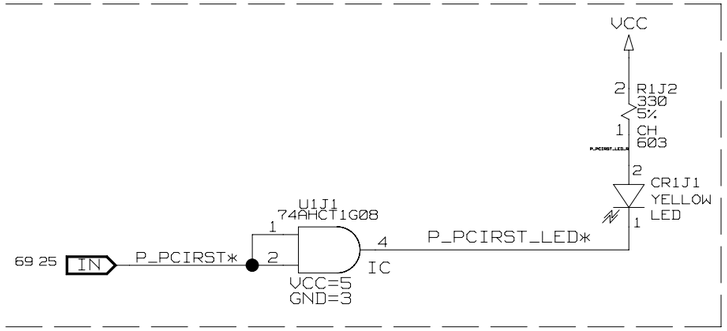
DRAWING

FAB_A.SCH.1.73
Mon Nov 25 12:50:15 2002
D845GFT FAB_A

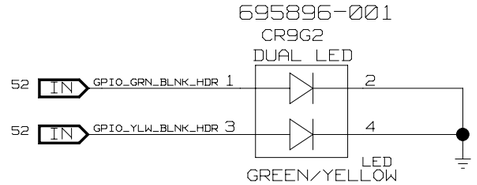
	DOCUMENT NUMBER	PAGE	REV
	C23021	73	4.0

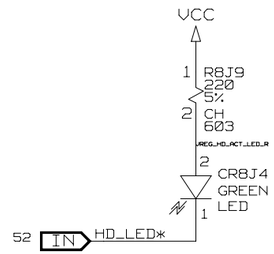
DEBUG/EV FEATURE: FRONT PANEL SWITCHES



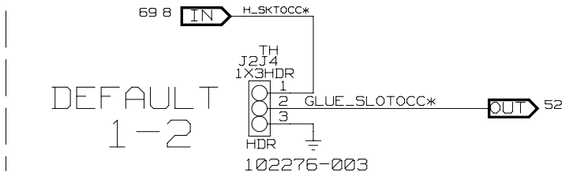


PRODUCT FEATURE: STATUS LED'S

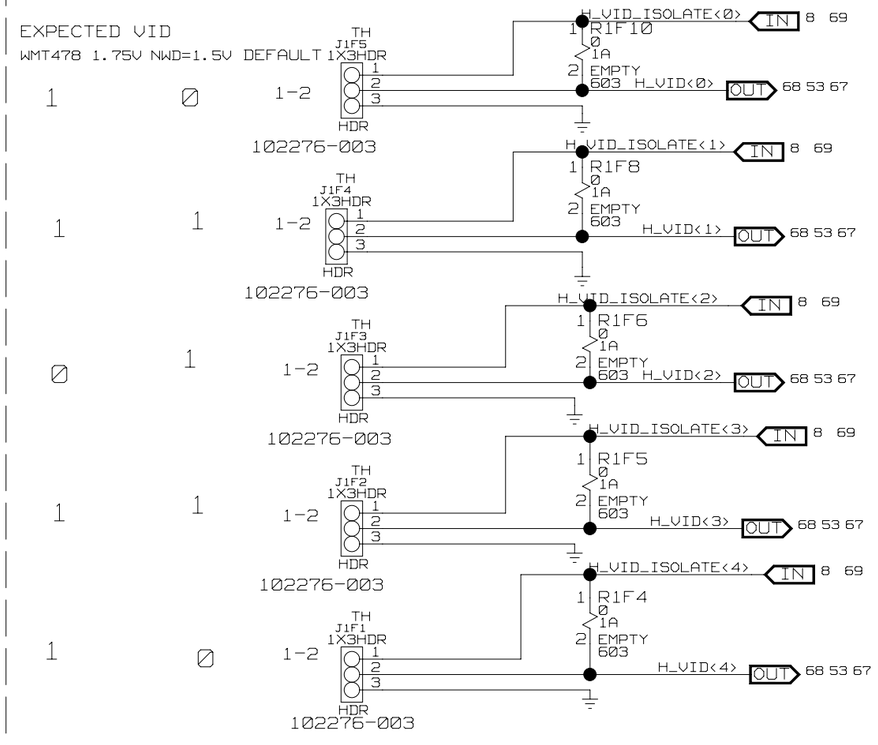




DEBUG/EV FEATURE: POWER-ON FORCING HEADER



DEBUG/EV FEATURE: VID JUMPERS

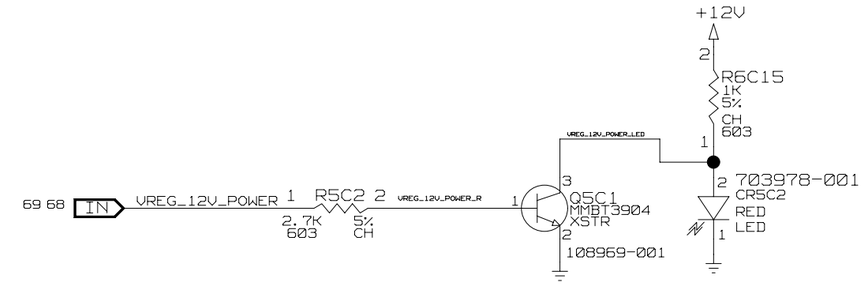


VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	1	1	1	1	OFF
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

DESIGN NOTE: VID JUMPER FUNCTION

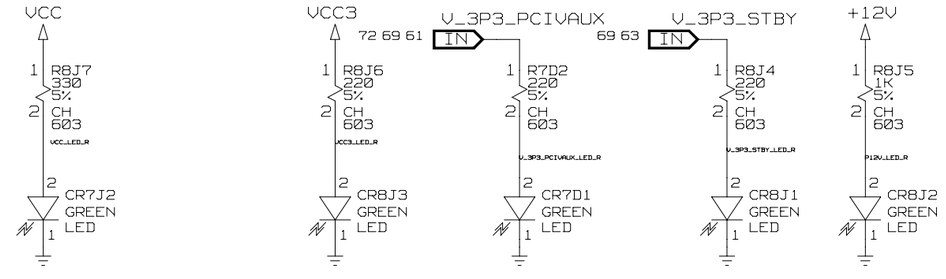
	JUMPER POSITION		
EV CARD?	1-2	2-3	REMOVED
YES	AVOID	FORCE 0	EV DRIVES
NO	CPU DRIVES	FORCE 0	FORCE 1

DEBUG/EV FEATURE: RED WARNING LED ON CPU 12V CONNECTOR



CAD NOTE: PLACE @ 2X2 CONNECTOR

DEBUG/EV FEATURE: POWER RAIL STATUS LED'S



DEBUG STUFFING OPTIONS: BOM=VREG_LED_DEBUG

[PAGE_TITLE=DEBUG_LED_DISPLAY]

DRAWING . FAB_A.SCH.1.74
Mon Nov 18 13:56:44 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	74	4.0

[FULL_ID=1164-84-16556] [PAGE_INFO_ID=16556] [MODULE_ID=1130-81-15288] [DONOR_ID=1130-81-15288]

SPARE

TP_RP1_240_1 — RP9H2 240 5% .063W IC SM (4 / 5) — TP_RP1_240_8

TP_RP2_240_1 — RP9H2 240 5% .063W IC SM (3 / 6) — TP_RP2_240_8

BLANK PART NUMBER: 3.3V COMPATIBLE (IPN XXXXXX-XXX)
PROGRAM FILE FROM D.E.SUBMITTED TO VENDOR
PROGRAM PART NUMBER & PLD-FA: A38794-001

EPM7032AETC44-10

44 PIN TQFP

U9J1

EPM7032 A38794-001

69 7 IN	CK_P_33M_PORT80	37	GCLK	
69 25 IN	P_PCIRST*	39	GCLR	
		38	OE1	
PORT80_OE1_OE2_PD		40	OE2	
IO32	44	L_FRAME*	IN	24
IO31	43	TP_PORT80_UNUSED_43		
IO30	42	TP_PORT80_UNUSED_42		
IO29	35	TP_PORT80_LED_RESET_35		
IO28	34	LED_HI_OUT1	OUT	75
IO27	33	LED_HI_OUT2	OUT	75
IO26	32	TP_PORT80_TDO_32		
IO25	31	TP_PORT80_UNUSED_31		
IO24	30	TP_PORT80_UNUSED_30		
IO23	28	TP_PORT80_UNUSED_28		
IO22	27	TP_PORT80_UNUSED_27		
IO21	26	TP_PORT80_TCK_26		
IO20	25	LED_HI_OUT0	OUT	75
IO19	23	LED_LO_OUT1	OUT	75
IO18	22	LED_LO_OUT0	OUT	75
IO17	21	LED_HI_OUT6	OUT	75
IO16	20	LED_HI_OUT4	OUT	75
IO15	19	LED_HI_OUT5	OUT	75
IO14	18	LED_HI_OUT3	OUT	75
IO13	15	LED_LO_OUT6	OUT	75
IO12	14	LED_LO_OUT2	OUT	75
IO11	13	LED_LO_OUT5	OUT	75
IO10	12	LED_LO_OUT3	OUT	75
IO9	11	LED_LO_OUT4	OUT	75
IO8	10	TP_PORT80_UNUSED_10		
IO7	8	TP_PORT80_UNUSED_8		
IO6	7	TP_PORT80_TMS_7		
IO5	6	L_AD<3>	IN	24 46 51
IO4	5	L_AD<2>	IN	24 46 51
IO3	3	L_AD<1>	IN	24 46 51
IO2	2	L_AD<0>	IN	24 46 51
IO1	1	TP_PORT80_TDI_1		

1 — 202285-025 — R9J1 100 5% CH 603 — 2

IC

VCC<PQFP>=9,17,29,41
GND<PQFP>=4,16,24,36
NC<PQFP>=45

VCC=VCC3<~PORT80DEC>

CAD NOTE: ORIENT TO LEFT

DS9J1

LED_DISPLAY_10P

75 IN	LED_HI_OUT0	LED_HI_OUT0_R	1
75 IN	LED_HI_OUT1	LED_HI_OUT1_R	10
75 IN	LED_HI_OUT2	LED_HI_OUT2_R	8
75 IN	LED_HI_OUT3	LED_HI_OUT3_R	5
75 IN	LED_HI_OUT4	LED_HI_OUT4_R	4
75 IN	LED_HI_OUT5	LED_HI_OUT5_R	2
75 IN	LED_HI_OUT6	LED_HI_OUT6_R	3
		TP_PORT80_HI_7	7
		A	
		B	
		C	
		D	
		E	
		F	
		G	
		DP	
		ANODE	6 ▷ VCC3
		ANODE	9 ▷ VCC3

RP9J3 (2 / 7, 4 / 5) RP9J3 (1 / 8) RP9H2 (1 / 8) RP9J2 (3 / 6, 4 / 5) RP9J2 (2 / 7) — 240 SM 5% .063W

A30432-002 IC

ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT

DS9J2

LED_DISPLAY_10P

75 IN	LED_LO_OUT0	LED_LO_OUT0_R	1
75 IN	LED_LO_OUT1	LED_LO_OUT1_R	10
75 IN	LED_LO_OUT2	LED_LO_OUT2_R	8
75 IN	LED_LO_OUT3	LED_LO_OUT3_R	5
75 IN	LED_LO_OUT4	LED_LO_OUT4_R	4
75 IN	LED_LO_OUT5	LED_LO_OUT5_R	2
75 IN	LED_LO_OUT6	LED_LO_OUT6_R	3
		TP_PORT80_LO_7	7
		A	
		B	
		C	
		D	
		E	
		F	
		G	
		DP	
		ANODE	6 ▷ VCC3
		ANODE	9 ▷ VCC3

RP9J2 (1 / 8) RP9J3 (3 / 6) RP9J1 (2 / 7) RP9J1 (4 / 5) RP9H2 (2 / 7) RP9J1 (3 / 6) RP9J1 (1 / 8) — 240 SM 5% .063W IC

A30432-002 IC

CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY

VCC3 — C9J3 (1 / 2) .1UF 10% 16V X7R 603 — C9H6 (1 / 2) .1UF 10% 16V X7R 603

VCC3 — C9J2 (1 / 2) .1UF 10% 16V X7R 603 — C9J1 (1 / 2) .1UF 10% 16V X7R 603

DEBUG/EV FEATURE: PORT 80 DECODER & DISPLAY

[PAGE_TITLE=LPC_DEBUG_PORT_80]

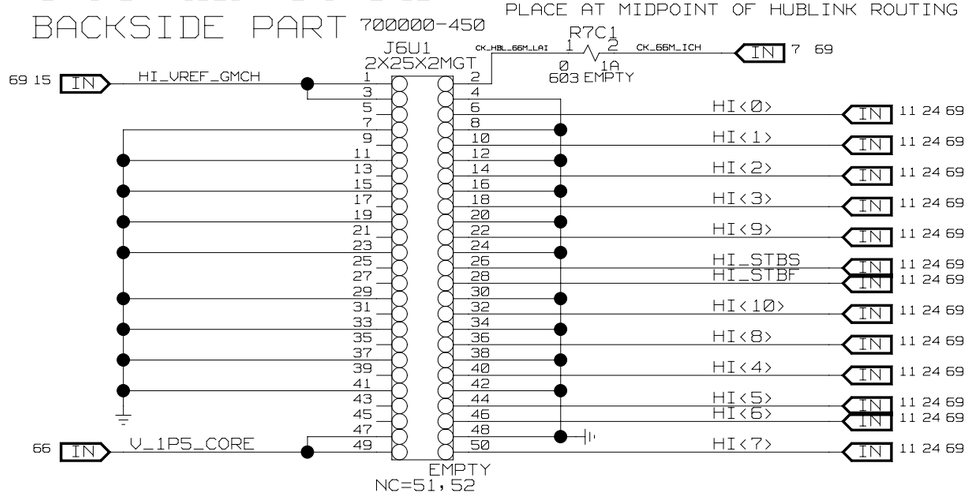
DRAWING
FAB_A.SCH.1.75
Mon Nov 18 13:56:54 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	75	4.0

DEBUG/EV FEATURE: HUBLINK LAI HEADER

NOTE: BACKSIDE PART 700000-450

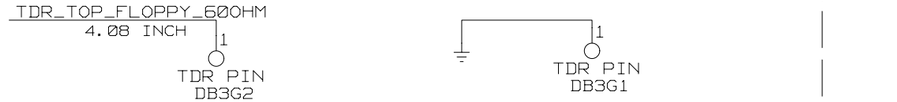
PLACE AT MIDPOINT OF HUBLINK ROUTING



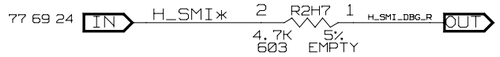
SOLDER MASK PADS: 5, 9, 13, 17, 21, 25, 27, 31, 35, 39, 43, 45

PINS ARE NOT ASSIGNED TP SIGNAL NAMES (PREVENTS TRACE CONNECTION)

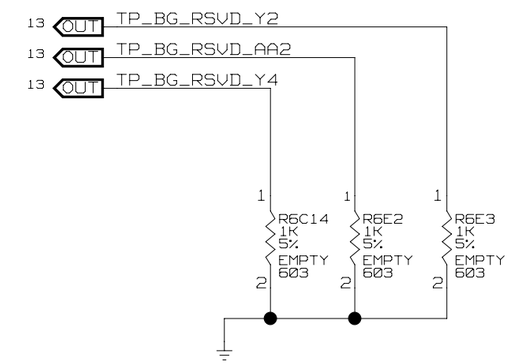
DEBUG/EV FEATURE: TDR COUPONS



DEBUG/EV FEATURE: INVERTING LEVEL SHIFTERS ON FSB SIGNALS FOR DIAG LED'S

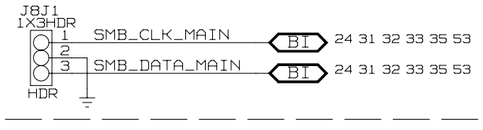


DEBUG/EV FEATURE: GMCH PILOT MODE STRAPS.



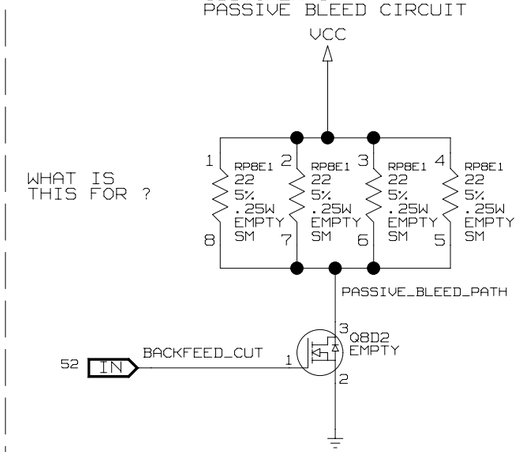
	GMCH PIN #
PILOT_8	Y8
PILOT_7	AA4
PILOT_6	W7
PILOT_5	AA5
PILOT_4	AA3
PILOT_3	Y4
PILOT_2	AA2
PILOT_1	Y2
PILOT_0	Y3

DEBUG/EV FEATURE: SMBUS LAI HEADER

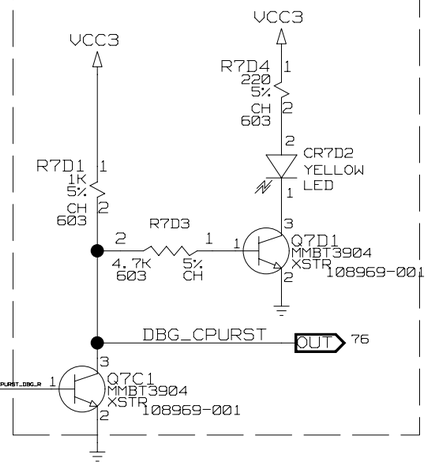


CUSTOMER C PASSIVE BLEED CIRCUIT

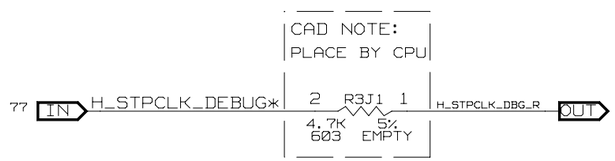
WHAT IS THIS FOR ?

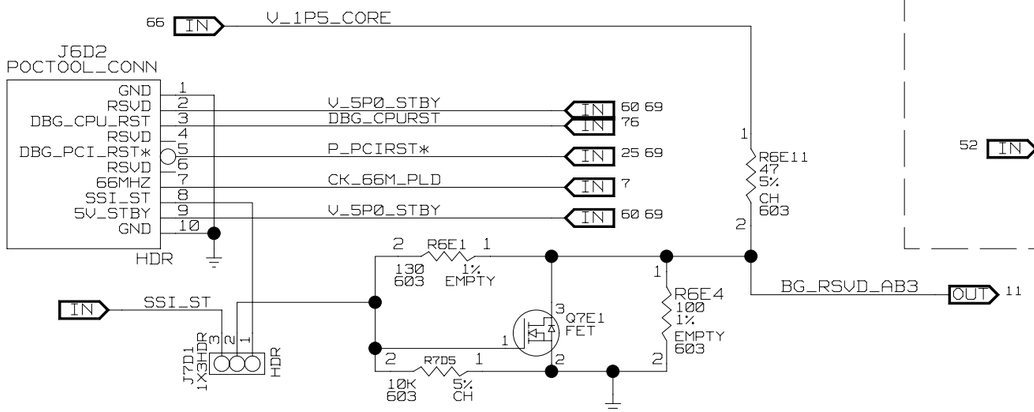


CAD NOTE: PLACE UNDER DIMMS

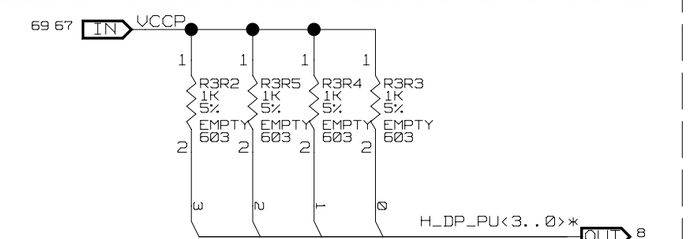


CAD NOTE: PLACE BY CPU





DEBUG/EV FEATURE: BACKSIDE RESISTIVE TEST LOAD SITES



CAD NOTE: PLACE ON BACKSIDE, KEEP DP TRACE SHORT

DRAWING FAB_A.SCH.1.76
Mon Nov 18 13:57:06 2002
D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	76	4.0

10 IN H_VCCA

R3C3 0 1A EMPTY 603 (2 / 1)

10 IN H_VCCIOPLL

7 IN CK_CPU_PCI_STOP

C6B10 1.0UF 10% 10V X5R EMPTY 603 (1 / 2)

DEBUG/EV FEATURE: GPIO STRAPS

VCC3

R1H7 4.7K 603 5% CH (1 / 2)

GP20_STRAP OUT 46

R1H6 470 603 5% EMPTY (1 / 2)

VCC3

R1H5 4.7K 603 5% CH (1 / 2)

GP21_STRAP OUT 46

R1H4 470 603 5% EMPTY (1 / 2)

DEBUG/EV FEATURE: GMCH TEST MODE STRAP

R6E5 4.7K 603 5% EMPTY (2 / 1)

BG_RSVD_AB2 OUT 11

DEBUG/EV FEATURE: SMI/STPCLK INJECTION HEADERS

DEFAULT JUMPER 1-2

J2J1 1X2HDR 102276-001 EMPTY (1 / 2)

H_SMI_INJECT*

603 EMPTY 100 5%

24 IN ICH_H_SMI* R2H6 0 603 1A EMPTY (2 / 1) R2H9 100 603 EMPTY 5% (1 / 2) R2H5 0 603 1A EMPTY (2 / 1) H_SMI* OUT 24 69 8 76

DEFAULT NO JUMPER

J2J2 1X2HDR EMPTY 102276-001 (1 / 2)

JMPR_SMI_OUT_PD* R2J2 4.7K 603 5% EMPTY (2 / 1)

Q2J1 MMBT3904 EMPTY (3 / 1 / 2)

108969-001

DEFAULT JUMPER 1-2

J3J1 1X2HDR 102276-001 EMPTY (1 / 2)

H_STPCLK_INJECT*

603 EMPTY 100 5%

24 IN ICH_H_STPCLK* R3H9 0 603 1A EMPTY (2 / 1) R3H10 100 603 EMPTY 5% (1 / 2) R3H7 0 603 1A EMPTY (2 / 1) H_STPCLK* OUT 24 69 8

R3J2 0 1A EMPTY 603 (2 / 1)

H_STPCLK_DEBUG* OUT 76

DEFAULT NO JUMPER

J3J2 1X2HDR EMPTY 102276-001 (1 / 2)

JMPR_STPCLK_OUT_PD* R3J3 4.7K 603 5% EMPTY (2 / 1)

Q3J1 MMBT3904 EMPTY (3 / 1 / 2)

108969-001

DEBUG FEATURE

R7B3 0 603 1A EMPTY (2 / 1)

OSC_CK14M_XTALIN OUT 7

OSC_CK14M_XTALIN_SMA

INSTALL ONLY IF XTAL IS REMOVED ON CK08

R7B2 49.9 1% EMPTY 603 (1 / 2)

63 IN V_1P5_STBY R7U1 0 402 5% EMPTY (1 / 2) V_1P5_STBY IN 63

ICH4 E20 BYPASS

15 IN GMCH_GTLREF R5R1 0 402 5% EMPTY (1 / 2) GMCH_GTLREF IN 15

9 IN CPU_GTLREF R3R1 0 402 5% EMPTY (1 / 2) CPU_GTLREF IN 9

[PAGE_TITLE=DEBUG_HEADERS]

DRAWING

FAB_A.SCH.1.77

Mon Nov 18 12:34:45 2002

D845GFT FAB_A

DOCUMENT NUMBER	PAGE	REV
C23021	77	4.0